

**CONTROL FIELD LISTING
MODEL 7201-02
COMPUTING ELEMENT
IBM 9020D/E SYSTEMS**

FIRST EDITION

SECOND PRINTING

7201-02

CE

CONTROL FIELD LISTING

AIRWAY FACILITIES BRANCH
FEDERAL AVIATION ADMINISTRATION ACADEMY

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1. The 7201-02 was the FAA version of the IBM S/360-65, with some additional features. In "360 Mode" it functions as a 2065 CPU.
2. "LADs" are Logic Automated Diagrams, similar to ALDs (Automated Logic Diagrams) but with miscellaneous information rather than logic circuits. LAD and ALD pages are both slightly larger than ISO A3.
3. The *CE Logic Index* (pp3-11) lists the various functional building blocks of the CPU (e.g. parallel adder) and the ALD page number that contains the logic circuits for that function. It also indicates in which ALD volume the pages reside.
4. The *Logout and Roller Index* (pp12-17) shows which logout word half (left and/or right) and front panel roller position are associated with the subject functional component, ordered by "topic".
5. A description of how to interpret *CAS Blocks* follows (pp18-23). Each ROS word is represented by a block on a Control Automation System (CAS) Logic Diagram (CLD). Each CAS block illustrates the actions of the control fields of one ROS word. Each CLD page (a type of ALD) can hold up to 72 CAS blocks, arranged as a micro-program flow chart.
6. The *CAS Index* (pp24-28) lists all valid CPU instructions and their (hex) op codes and shows which CAS ALD page the micro-program flowchart can be found on. Note that all CAS pages (and *only* CAS pages) begin with the letter "Q". Page 27 lists non-op code CAS pages.
7. Page 28 lists ROS addresses that are 'forced' by certain machine conditions, such as I/O Interrupt and Power On Reset (the first ROS address executed when the machine is powered on).
8. The *Micro-Order Index* (pp29-38) lists the symbolic micro-orders (as used in the CAS blocks) along with their "decode order", which is the ROS field and bit pattern. For example, the symbolic micro-order "ABC=7" is defined by J39 which is the bit pattern 0100111 in the "J" field (ROS bits 62-68).
9. The *Control Fields and Micro-Orders* listing (pp39-89) explains in detail what function every micro-order performs, and the ALD page number that contains the logic circuits for that micro-order function.
10. Fields D, F, and G are interpreted differently when the CPU is in *Scan Mode*. The last two pages of the *Control Fields and Micro-Orders* listing (pp88-89) describes this alternative meaning.

This manual is intended as an instructional aid for use by instructors and students at the FAA Academy.

The major part of this document is a direct extract from the Academy Model 7201-02 Compute Element LADs. Changes and additions have been made to clarify and correct the LADs where necessary.

CE LOGIC INDEX

<u>FUNCTION</u>	<u>VOLUME</u>	<u>ALD PAGE NOS</u>
A REG 00-31	24	RA001--RA301
AB REG INGATING	24	RB901--RB907
ABC-ABC-INCR. + CNTLS	07	CW011--CW051
ABC CNTR STEP	16	KZ501
AB--SIBA	24	RB733--RB803
ATR SLOT CONTROLS	10	FA001--FA141
ATR DECODE	18	MA701--MA741
ATR RECEIVERS	21	MP051--MP091
B REG 32-67	24	RB321--RB671
BUC CLEAN UP	20	MC711
BLOCK I-FETCH	12	KD501
BLOCK INTERRUPTS	15	KW021
BLOCK TGR	15	KW041
BLOCK ROSAR RESET	27	RX003
BRANCH INVALID ADDRESS	12	KD701
CCR 001-31	10	FC001--FC305
CCR CONTROLS	10	FC311--FC351
CCR PARITY CK	10	FC361
CE TO CE INTERFACE	11	FX491--941
CE TO SE + DE SIMPLEX CABLES	28	WA150--WA160
CE LOG REQUEST + HARDSTOP	15	KW071
CHECK RESPONSE TRIGGER	16	KX311
CLOCK CONTROLS + RESETS	12	KC011--KC101
CLOCK POWERING	04	AP001--AP021
CLOCK DISTRIBUTION	06	AS201
CONDITION CODE REG	27	RW341--RW352
CONSOLE		
DRIVERS TO SYS CONSOLE	21	PX501--PX561
INDICATORS--ALL--	21	PL011--PL061
INTERRUPT	12	JA201

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<u>FUNCTION</u>	<u>VOLUME</u>	<u>ALD PAGE NOS</u>
SWITCHES (CE)	21	PK001--PK061
SWITCHES (SC)	21	PX011--PX451
CPU TO STORAGE SIMPLEX CABLES	28	WA021--WA031
D REG (INDICATED 08-31)	24	RD001--RD220
D REQUEST	20	MC061
DAR REG 00-30	10	FD001--FD301
DAR CONTROLS	10	FD951
DAR INTERRUPTS	10	FD931--FD941
DAR INTERRUPT TRIGGER	12	JA251
DAR MASK REG 00-31 + P	10	FD501--FD921
DCT CE-CE SIMPLEX CABLES		WA201--WA202
DISABLE INTERLEAVE + REV STOR	15	KU031
E REG		
00-15	25	RE001--RE941
PARITY CK	25	RE181
INCREMENTER	07	CE081--CE181
INCREMENTER CONTROL	07	CE901--CE961
EDIT CONTROL	16	KZ011--KZ501
EXCEPTL CONDITION I-FETCH	12	KMB11--KM861
EXECUTE TRIGGER	12	KD601
EXTERNAL REG 00-31 + P	11	FE001--FE331
EXTERNAL BUS CABLES	28	WA211--WA281
F REG		
00-07 + P	25	RF001--RF081
REG DECODE	25	RF101
SWITCH CARDS (INPUT)	25	RF701
CONTROLS	25	RF801--RF901
FETCH DATA CK	20	MC941
FLT ROS LOGOUT CONTROL	15	KU201--KU241

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<u>FUNCTION</u>	<u>VOLUME</u>	<u>ALD PAGE NOS</u>
FLT INTERFACE SELECT	15	KU281
FLT PASS-FAIL TGRS	15	KU391
FLT IPL LTH	15	KW501
FLT TEST LTH	15	KU291
FORMAT CONTROL	29	XM001--XM006
FORMAT DECODE	29	XM901--XM905
G REG 00-07 + P	25	RG001--RG051
GATED OSC	12	KC101
IC REQUESTS	20	MC066
INDICATORS (ALL)	13+14	KT001--KT571
I-FETCH	12	KD101--KD901
I-FETCH REQUEST	12	KD701
I-FETCH INVALID ADDRESS	12	KD711
INHIBIT-STORAGE PROTECT TGR	20	MC181
INHIBIT LS WRITE	27	RX003
INSTRUCTION COUNTER		
00-23 (INDICATED 08-31)	07	CA001--CA215
PARITY	07	CA231--CA241
CONTROLS	07	CA901--CA911
GATES TO Padder	07	CA701
IN LSWR	13	KS321
INSTR LNTH NOT AVAILABLE	12	KM851
INTERRUPTS	12	KM121--KM861
INTERRUPT GATE TRIGGER	16	KX181
INTERRUPT PRIORITY TGR 1 + 2	13	KN121
IOCE CONTROLS	16	KX091--KX411
IOCE DIST SIMPLEX IF	11	FX091--FX441
IOCE SIMPLEX IF	16	KX131--KX152
IOCE I/O INTRPT REQ TGRS	12	KM311--KM331

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<u>FUNCTION</u>	<u>VOLUME</u>	<u>ALD PAGE NOS</u>
IOCE MCK INTRPT REQ TGRS	12	KM331
IOCE DISTR SIMPLEX CABLES		WA311--WA321
IPL SYS-SUBSYS	15	KW321
INSERT KEY TGR	20	MC181
K REG 00-31	25	RK001--RK341
LAL 00-04	17	LS801--LS821
LAR 00-04	17	LS851--LS881
LEAVE TRIGGER	16	KZ201
LM REG 00-63 + P	28	XL001--XL661
LM--N BUSS	28	XL661--XL741
LOCAL STORE		
9020 BUS IN 00-31	06	BF001--BF315
9020 BUS IN PARITY	06	BF401--BF441
9020 BUS REVR + TERMS	06	BF501--BF671
9020 REGS GATE POWERING	06	BF701--BF731
BITS 00-31	17	LS001--LS317
CONTROLS + DECODE	17	LS401--LS991
LOG OUT ADR ERROR	18	MA901
LOG OUT ROS CHECK	15	KU231
MAINT MODE STOP CLOCK	15	KU251
MANUAL CONTROLS	15	KW005--KW501
MANUAL TGR	15	KW031
MARK TRIGGERS + P	07	CT011--CT051
MCW 00-51	15	KU001--KU091
MCK INTERRUPT		
CE	12	KM121
IOCE	12	KM331
MICRO ORDER BRANCH DECODE	08	DS011--DS365
MICRO ORDER DECODE	08	DR011--DR211
MIXER	29	XM021--XM635

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<u>FUNCTION</u>	<u>VOLUME</u>	<u>ALD PAGE NOS</u>
MODE TGRS		
INSTRUCTION STEP	15	KW021
PULSE	15	KW061
SINGLE CYCLE	15	KW021
360	15	KW301
WRAP	08	DT061
SCAN	08	DR211
FLT	15	KU291
ROS TEST	15	KU331
MULTIPLY DECODE + CONTROL	07	CT011--CT051
MULTIPLY DECODE SELECT	07	DP031--DP071
N REG 00-15 + P	29	XN001--XN301
NO RETRY	13	KS321
OBS OTC IOCE	12	KM371
OPERATION DECODE	07	DN091--DN121
OSC CLOCK SHAPING + DISTR	12	KC011
PAGING		
NEW ADDRESS D	24	RD301--RD321
NEW ADDRESS IC	07	CA911
LTHS + EXCEPTION	20	MC991--MC997
PARALLEL ADDER		
00-63	04+05	AP041--AP631
64-67	04	AP671--AP675
A SIDE BUS		RT701--RT747
A SIDE CONTROL		RT801--RT823
A SIDE PARITY		RT771--RT777
A SIDE BUS	24	RB805--RB817
B SIDE PARITY	24	RB755--RB761
B SIDE CONTROL	24	RB701--RB811

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<u>FUNCTION</u>		<u>VOLUME</u>	<u>ALD PAGE NOS</u>
FULL SUM CHECK	04-07	04	AP075
	08-15	04	AP154
	16-23	04	AP234
	24-31	04	AP314
	32-39	04	AP394
	40-47	04	AP474
	48-55	05	AP554
	56-63	05	AP634
	64-67	05	AP675
HALF SUM CHECK	56-67	05	AP751
	40-55	05	AP761
	24-37	05	AP771
	08-23	05	AP781
	04-07	05	AP791
GATE TO IC		07	CA901
GATE TO D		27	RT913
PASS PULSE TGR		15	KW041
Q REG + CONTROLS		25	RQ001--RQ921
PAM OR RCU INTERFACE		11	FX001--FX021
PAM OR RCU CABLES		28	WA401
PGM INTERRUPT CONTROLS		12	KM171--KM301
PGM INTERRUPT LATCH		12	KM161
PGM STORE COMPARE		12	KD501
PGM INTRPT TGRS	01-02	12	KM141
	04-08	12	KM151
	16-32	12	KM156
	64-128	12	KM158
PIR REQUEST		12	KM381--KM391
PIR INTRPT TGR		12	JA251
PROSA A-B		27	RX201--RX241
PSA LOCKOUT IOCE		12	KM341--KM351
PSBAR		21	MP111--MP551

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<u>FUNCTION</u>	<u>VOLUME</u>	<u>ALD PAGE NOS</u>
PSW 00-39	27	RW011--RW381
PSW 20-31--ST	13	KN211--KN311
PSW RESTART SYS-SUBSYS	15	KW321
R REG 00-15 + P	26	RR001--RR161
READ + WRITE DIRECT	12	JA001--JA901
EXT START + STOP	12	JA301--JA311
EXT INTRPT TGRS	12	JA201--JA241
CONTROLS + RCVRS + CLOCK	12	JA001--JA081
RELEASE CPU	16	KX411
REPEAT INSTRUCTION	15	KW051
REPEAT ROS ADDRESS	27	RX901
REPEAT ROS TEST	15	KU211
RESET 9020 FUNCTIONS	15	KW411
RESTART ROS TIMER	12	KM361
RETRY	12	KM321
ROS MICRO ORDER DECODE	08	DR011--DS481
ROSAR	27	RX021--RX111
ROSDR + LTHS + P	27	RY011--RY141
S REG 00-31 + P	26	RS001--RS315
S REG MPR BUS	07	DP011--DP012
S BUS 00-31	07	DP021--DP022
S REG MPR PTY CK	07	DP091
S TGR	16	KZ321
SAB	18	MA001--MA601
SAB PARITY CHECK	18	MA901--MA961
SAB CABLE ROUTING	28	WA001--WA011
SATR DECODE	10	FA501--FA551
SC DISTR SIMPLEX CABLES	28	WA611--WA643
SCAN CTR AND ADDRESS SEQ	15	KU101--KU191
SCAN IN POWERING	15	KU191

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<u>FUNCTION</u>	<u>VOLUME</u>	<u>ALD PAGE NOS</u>
SCAN OUT BUS PREORS	14	KT801--KT991
SCAN OUT WORDS	14	KT601--KT771
SCAN CLOCK	15	KW271
SCAN CONTROLS	15	KU331--KU591
SCAN REQUEST	20	MC068
SCON AND SATR CONTROLS	13	KR001--KR211
SCU CABLES	28	WA501
SCU DRIVERS RCVRS	11	FX053--FX057
SDBI SDBO	19	MB001--MB995
SDBI SDBO CABLES	28	WA170--WA140
SELECT REG 00-32 + P	11	FS001--FS531
SELECT TIMING PULSE	20	MC707
SE SIMPLEX CABLES	28	WA150--WA160
SET KEY TGR	20	MC181
SOROS TGR	15	KU351
SERIAL ADDER 00-07 + P	06	AS001--AS081
A SIDE BUS	05	AR001--AR082
A SIDE CONTROL	05	AR101--AR421
B SIDE BUS	05	AR501--AR601
B SIDE CONTROL	05	AR801--AR901
B SIDE BUS FM ST	27	RT751--RT771
ERRORS	06	AS095
SE STOPPED	12	KM181
SE VALID	21	MPO01--MPO41
SPLIT LOGOUT TGR	20	MC791
STATUS TGRS AND CNTLS	13	KS021--KS321-AS105
STC TGR INCREMENT CTR	07	CS011--CS061
STORAGE CHECKS	20	MC756
STORAGE SELECTS	20	MC551--MC601
STORAGE TIMEOUT	20	MC753
STORAGE LOGOUT POWERING	15	KU611
STORAGE LOGOUT + LOGOUT STOP	15	KU601--KU641

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<u>FUNCTION</u>	<u>VOLUME</u>	<u>ALD PAGE NOS</u>
STORAGE ID LTHS	20	MC961
STOP TGR	15	KW031
STOP CPU CLOCK TGR	20	MC271
T REG 32-63 + P	27	RT321--RT661
TAU CABLES	28	WA501
TAU RCVRS	11	FX031--FX051
TIC LATCH	15	KU291
TIME CLOCK AT LIMIT	12	KM221
TIME CLOCK STEP	12	KD601
TIMING GATE TGR	16	KX311
TX TGR	07	DP071
WAIT STATE BLOCK ROS CLOCK	27	RX002
WRAP	08	DT001--DT121
WRAP SMPLX + MLTPLX CABLES	28	WA700--WA710
XY REG 00-63 + P	29	XX001--XX651
XY REG PARITY PREDICT	29	XM007--XM018
Y BRANCH DECODE	08	DS261
Z BRANCH DECODE	08	DS101--DS108

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LOGOUT AND ROLLER

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<u>TOPIC</u>	<u>SUBJECT</u>	<u>LOGOUT WORD</u>	<u>ROLLER/POS</u>
CHECKS	ATR PARITY	5L	6/5R
	CCR PARITY	5L	6/5R
	E REG PARITY	13L	2/2L
	IOCE BUS	5L	6/5R
	LOCAL STORE BUS	5L	6/5R
	LOGOUT ADDRESS	5L	6/5R
	ROS	5L	6/5R
	PARALLEL ADDER FULL SUM	12R	2/2R
	HALF SUM	12R	2/2L
	PSBAR ALTERNATE	5L	6/5R
	NOT CONFIGURED	5L	6/5R
	PARITY	5L	6/5R
	READ DIRECT TIME OUT	5L	6/5R
	ROS PARITY	12R	2/2R
	SERIAL ADDER FULL SUM	12R	2/2R
	HALF SUM	12R	2/2R
	SPLIT LOGOUT	5L	6/5R
	SAB	5L	6/5L
	SDBI	5L	6/5L
	SDBO	5L	6/5L
	S.E. ADDRESS	5L	6/5L
	DATA	5L	6/5L
	TIME OUT	5L	6/5L
STORAGE LOGOUT	5L	6/5L	
CONFIGURATION CONTROL	ATR	2L, 3L	1/1R, 2/1
	CE SEL ATR	1L, 2L	1/1L
	CCR	8R	5/5
	PSBAR	8L	5/1

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<u>TOPIC</u>	<u>SUBJECT</u>	<u>LOGOUT WORD</u>	<u>ROLLER/POS</u>
COUNTERS	ABC	6R	6/2R
	FLT	5R	5/2L
	PSBAR	8L,13L	5/1L
	STC	6R	6/2R
EDIT	RIGHT DIGIT TGR	15R	4/4R
	S TGR	15R	4/4R
	LEAVE TGR	15R	4/4R
	STEP ABC TGR	15R	4/4R
INSTRUCTION FETCH CONTROLS	BLOCK I FETCH TGR	3R	4/5L
	I FETCH 1 TGR	1L	4/5L
	2 TGR	3R	4/5L
	3 TGR	3R	4/5L
	REQ TGR		
	INVALID ADDRESS TGR	3R	4/5L
	BRANCH INVALID ADDRESS TGR	3R	4/5L
	EXECUTE	3R	4/5L
	PROGRAM STORE COMPARE	3R	4/5L
INTERRUPTS	EXTERNAL	1L,3R	4/5R
	PROGRAM	3R,8L,	4/5R,5/1R
	INTERRUPT PRIORITY		
	GATE TGR	2L	3/5L
IOCE CONTROLS	LOGOUT	1R	3/5L
	PERMIT	1R,13L	3/5L
	SELECT	2L	3/5L
	MACH CHECK INTR REQUEST	2L	3/5L

LOGOUT AND ROLLER

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<u>TOPIC</u>	<u>SUBJECT</u>	<u>LOGOUT WORD</u>	<u>ROLLER/POS</u>
LOCAL STORE	LAR	19R	6/2L
	INHIBIT LS WRITE	19R	6/2L
	WRITE LS	19R	6/2L
MANUAL CONTROLS	BLOCK INTR	4R	3/1L
	BLOCK TGR	4R	3/1L
	CHECK SUM	4R	3/1R
	CLOCK INHIBIT	4R	3/1R
	FORCE ADDRESS	4R	3/1L
	PASS PULSE	4R	3/1L
	PULSE MODE	4R	3/1L
	REPEAT INSTRUCTION	1L,4R	3/1L
	SINGLE CYCLE	4R	3/1R
	STOP TGR	4R	3/1L
TEST SWITCH	5L	6/5L	
MAINTENANCE CONTROL WORD	MCW BITS 1-7	5R	5/2L
	32-51	20R	6/6
MISC	CONSOLE SIGNAL	3R	4/5R
	GATE CONTROL TRIGGERS	14R,19R	5/4
	NO RETRY	13L	4/1R
	OSC INHIBIT	2L	1/1L
	TIME GATE TGR	3R	4/5R
	TX TGR	6R	6/2L
	360 MODE	5L	6/5L
PROGRAM STATUS WORD (PSW)	PROGRAM INTERRUPTS	4L,BL,	4/1R,5/1R
	MASK	4L	4/1
	PROTECTION KEY	4L	4/1L
	SYSTEM MASK	4L,8L	4/1L,5/1R
	IC	9R	6/3

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<u>TOPIC</u>	<u>SUBJECT</u>	<u>LOGOUT WORD</u>	<u>ROLLER/POS</u>
REGISTERS	AB BITS 00-67	6R,7	6/2R,3/3,4/3
	PARITY	1R	3/3,4/3
	ATR BITS 00-39	2L,3L	1/1R,2/1
	PARITY	1L	1/1R,2/1
	CCR BIT 00-31	8R	5/5
	PARITY	0R	5/5
	D BITS 08-31	10R	1/2
	PARITY	0L	1/2
	DAR BITS 00-31	12L	6/4
	DAR MASK BITS 00-31	9L	5/6
	PARITY	0L	5/6
	E BITS 00-15	10L	5/3R
	PARITY	1R	5/3R
	EXTERNAL BITS 00-31	6L	4/6
	PARITY	2L	4/6
	F BITS 00-07	10R	1/2L
	PARITY	0L	1/2L
	G BITS 00-07	2L	1/1R
	PARITY	1L	1/1R
	IC BITS 08-31	9R	6/3
	PARITY	13L	6/3
	K BITS 00-31	20L	2/6
	PARITY	18L	2/6
	LM BITS 00-63	21	1/6
	PARITY	18L,19L	1/6
	N BITS 00-15	19L	3/5R
	PARITY	13L	3/5R
	PSBAR BITS 08-19	8L	5/1
	PARITY	13L	5/1
	Q BITS 00-63	11	3/2,4/2
PARITY	0L	3/2,4/2	

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<u>TOPIC</u>	<u>SUBJECT</u>	<u>LOGOUT WORD</u>	<u>ROLLER/POS</u>
	R BITS 00-15	10L	5/3L
	PARITY	1R	5/3L
	SEL BITS 00-31	2R	1/5
	PARITY	0R	1/5
	ST BITS 00-63	23	1/3,2/3
	PARITY	0R	1/3,2/3
	XY BITS 00-63	22	2/5,3/6
	PARITY		
ROS	PREVIOUS ADDRESS A	16R	3/4R
	PROSA	18R,19R	1/4
	PROSB	18R,19R	1/4R
	ROSAR	18R,19R	1/4L
	ROSDR 02-35	17R,19R	2/4
	36-68	16R,19R	3/4
	69-99	15R,19R	4/4
	PARITY	17R,15R	2/4R,4/4
SCAN CONTROLS	ADDRESS SEQUENCER	5R	5/2L
	BACKSPACE	4R	3/1R
	BUFFER I	5R	5/2R
	CONSOLE LOGOUT	4R	3/1R
	DIAGNOSE	4R	3/1R
	DISABLE INTERLEAVING AND REVERSE STORAGE ADDRESS	1L,4R	3/1R
	FAIL	5R	5/2R
	FLT MODE	16R	3/4R
	TEST	4R	3/1R
	GAP	4R	3/1R
	MMSC	5R	5/2R
	PASS	5R	5/2R
	RELEASE	4R	3/1R

LOGOUT AND ROLLER
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<u>TOPIC</u>	<u>SUBJECT</u>	<u>LOGOUT WORD</u>	<u>ROLLER/POS</u>
	REPEAT TEST	4R	3/1R
	ROS TEST SEQUENCER	5R	5/2R
	TRIGGER	4R	3/1R
	SCC TRIGGER	4R	3/1R
	SOROS	4R	3/1R
	SYNC TRIGGER	4R	3/1R
	TIC	4R	3/1R
STATS	STAT A	1L	4/5L
	STAT B-H	3R	4/5L
STORAGE CONTROLS	CHECK ID	5L	6/5L
	INSERT KEY	4R	3/1L
	MARK TRIGGERS	6R	6/2L
	PAGE 1 LATCH	4R	3/1L
	REQUEST TRIGGERS	1L,4R	3/1L
	SET KEY	4R	3/1L
TIME CLOCK	AT LIMIT	3R	4/5R
	STEP	2L	1/1L

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INTERPRETATION OF CAS BOX DATA USING MICRO ORDER INDEX

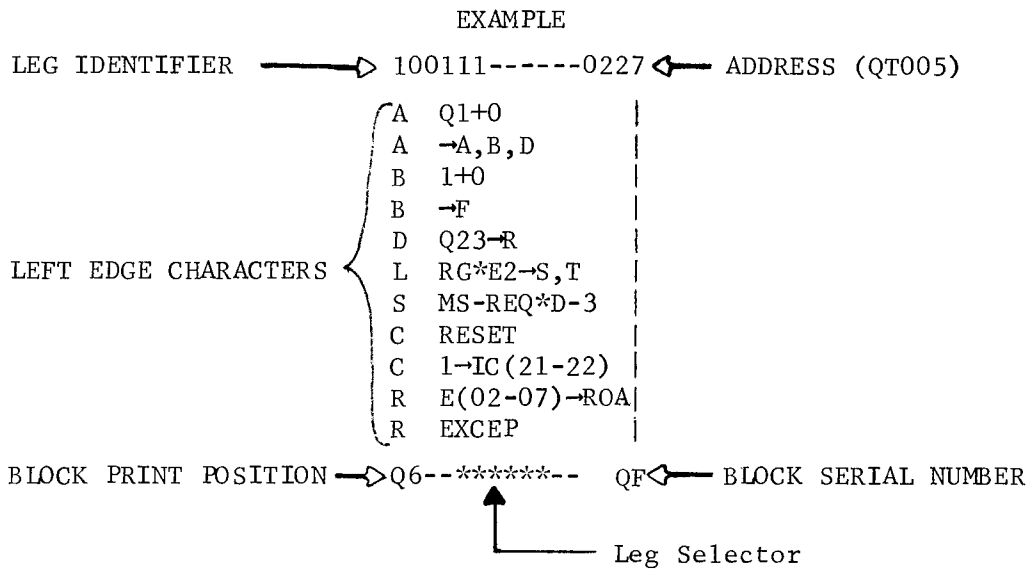


Figure 1

CAS SYMBOLS

+	True Add	Δ	9020 special micro-order
-	Complement Add (Subtract)	/	Non logical or
=	Is equal to	<	Is less than
→	Is set into	>	Is greater than
.	Logical and	¬	Not
*	Per (according to)	,	Non-logical Connective
≠	Is not equal to	∇	Exclusive or
Ω	Logical or	?	Dependent Serial Adder Functions

DEFINITIONS

- Leg Identifier : Branch address of this CAS block. For a detailed explanation, refer to CE Model 7201-02, Field Engineering Theory of Operation Manual (FETOM), page 1-20.
- Address : ROS word address.
- Box Print Position : Block position on the CAS page. Page is layed out in a grid system, consisting of horizontal rows of blocks labled A, C, E, G, J, L, N, and Q, top of page to bottom. Vertical block column assignments are from 1 through 9, left to right. In the example at the top of page 18, the block is located in horizontal row Q, vertical column 6.
- Block Serial Number : The two letter block serial number is composed of block horizontal row designation and letter representation of vertical column; where column 1 = A, column 2 = B, etc.
- Leg Selector : A field of 2 or 6 positions which define the branching conditions of the block (next ROS word address). A 6 position field defines a functional branch, and a two position field defines a X and Z branch. See FETOM, page 1-20.

Symbols used within a position are:

- X Don't care (may be 0 or 1; no effect).
- * Value of position (0 or 1) dependent upon micro-order tested conditions.
- 1 Position is unconditionally set to 1.
- 0 Position is unconditionally reset to a 0.
- Blank Position is unused.

Left Edge Characters: Define the data paths, addressing, functions, and control operations that are affected by micro-orders in the line.

INTERPRETATION OF CAS BOX DATA USING MICRO-ORDER INDEX

EDGE CHARACTERS AND THEIR MEANINGS ARE LISTED BELOW.

<u>EDGE CHARACTER</u>	<u>MEANING</u>
A	PARALLEL ADDER INPUTS (T,U,Q or V,U,Q)
A	PARALLEL ADDER LATCH CONTROL (P); PARALLEL ADDER OUTPUT DESTINATION(S)
B	CONSTANT OR N REG TO SERIAL ADDER INPUT BUSS B
B	SERIAL ADDER INPUTS
B	SERIAL ADDER OUTPUT DESTINATION (C,D); AB OR F REG BYTE TO SERIAL ADDER INPUT BUSS A (R)
D	MISC DATA TRANSFER INGATING CONTROLS
L	LOCAL STORE CONTROL SPECIAL REGISTERS TO LS BUSS, BUSS OUTGATING
S	MARK SETTING AND STORAGE REQUESTS
C	MISC CONTROLS
R	BRANCHING

INTERPRETATION OF CAS BLOCK NOTATION

Figure 1 is to be used to determine the actual mnemonics from the box data.

The two lines of edge character A completely define the action of the parallel adder during this cycle, and the two lines of edge character B define the serial adder. In each case, the first line defines the adder inputs. The second lines list the registers to which the adder latch output is to be gated during the next ingating time. In addition, the first character on the second A line may indicate a left or right shift at the adder latch input. Also, on the right side of the second B line, the choice of AB or F registers as serial adder input may be indicated.

As an example, the box shown as Figure 1 would be decoded as follows, using the micro-order index.

1. The first A line: Q1 is a field V mnemonic and looking it up in the control field listing, we see that it is a parallel adder input. +0 could be in either field M or field U, but U is the parallel adder input field. The mnemonics are Q1 (V7) and +0 (U0).
2. The second line statement → A, B, D may be broken up as follows:
 - is a P field mnemonic meaning set into the parallel adder latches (A edge character) without a shift (P0).
 - A,B is an A field mnemonic and looking it up in the control field listing (A3) defines it as an adder latch ingate to both registers A and B.
 - , is a non-logical connective meaning and.
 - D is a C field mnemonic with a C15 decode order. This ingate micro-order will take the contents of PAL bits 40-63 and ingate them into the D register.
3. The first B line: There are three possibilities for the mnemonic l, but only N15 is permissible on a B line. +0 on a B line must be M0.
4. The second B line: → is not part of the mnemonic here, but is automatically inserted meaning is set into. F is the D7 micro-order.

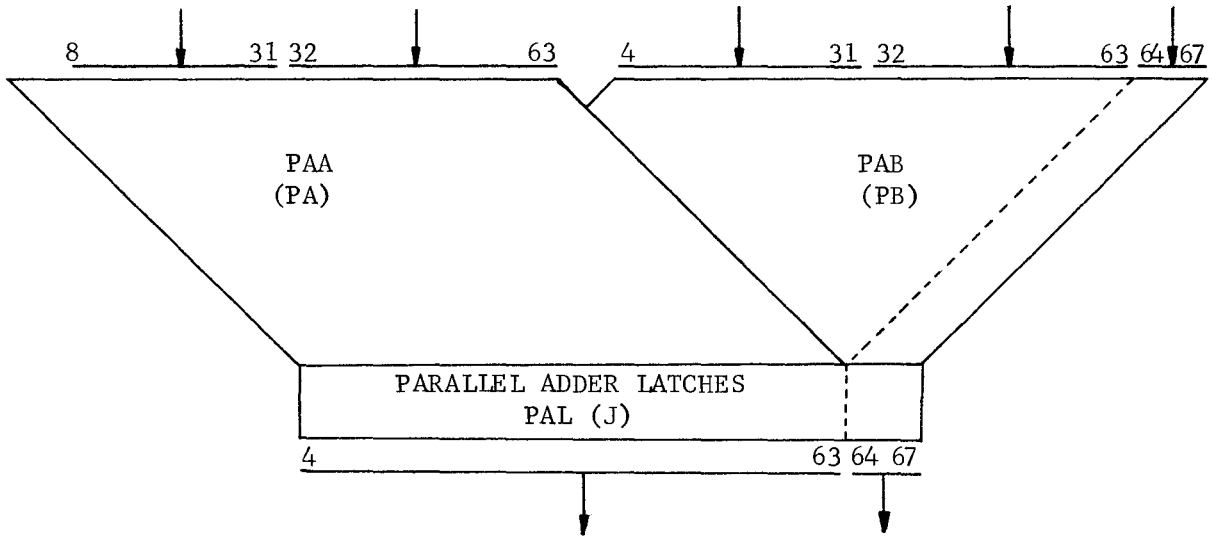
INTERPRETATION OF CAS BLOCK NOTATION

5. D line: Q23-~~R~~ is E13.
6. L line: RG*E2 is H14. → S,T is B3.
7. S line: MS-REQ*D-3 is L10.
8. The first C line: Reset is F1.
9. The second C line: 1-~~IC~~(21-22) is G17.
10. The first R line: E(02-07)-~~ROA~~ is J103.
11. The second R line: Excep is K25.

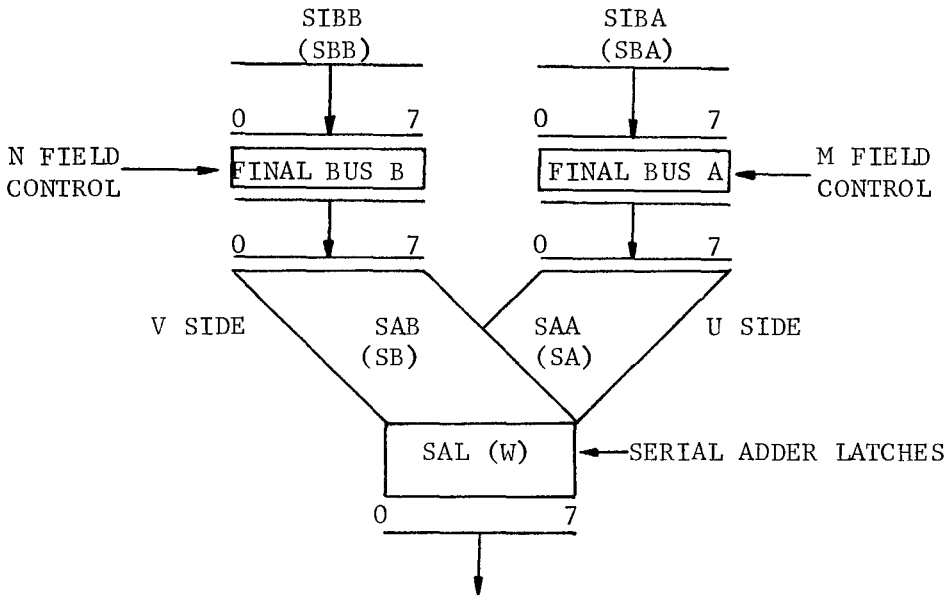
CAS LETTER DESIGNATIONS

NOTE: Letters within parenthesis are micro-order listing designations.

A. Parallel Adder (PADDR).



B. Serial Adder.



CAS INDEX

<u>MNEMONIC</u>	<u>OP CODE</u>	<u>CAS PAGE</u>	<u>MNEMONIC</u>	<u>OP CODE</u>	<u>CAS PAGE</u>
A	5A	QF001	CLC	D5	QP031
AD	6A	QG001	CLI	95	QK001
ADR	2A	QC061	CLR	15	QB001
AE	7A	QG001	CP	F9	QS001
AER	3A	QC001	CR	19	GB001
AH	4A	QB001	CSS	02	QQ201
AL	5E	QF001	CVB	4F	QE021
ALR	1E	QB001	CVD	4E	QE011
AP	FA	QS001	CVWL	03	QQ291
AR	1A	QB001			
AU	7E	QG001	D	5D	QB031
AUR	3E	QC061	DD	6D	QG001
AW	6E	QC061	DDR	2D	QC041
AWR	2E	QC061	DE	7D	QG001
			DER	3D	QC041
BAL	45	QE031	DIAG	83	QQ171
BALR	05	QE031	DLY	0B	QQ101
BC	47	QE041	DP	FD	QS041
BCR	07	QE041	DR	1D	QB031
BCT	46	QE041			
BCTR	06	QE041	ED	DE	QP041
BXH	87	QE031	EDMK	DF	QP041
BXLE	87	QE031	EX	44	QE051
C	59	QF001	HDR	24	QC001
CD	69	QG001	HER	34	QC001
CDR	29	QC061	HIO	9E	QK021
CE	79	QG001			
CER	39	QC061	IATR	0E	QQ101
CH	49	QB001	IC	43	QE001
CL	55	QF001	ISK	09	QJ031

CAS INDEX

<u>MNEMONIC</u>	<u>OP CODE</u>	<u>CAS PAGE</u>		<u>MNEMONIC</u>	<u>OP CODE</u>	<u>CAS PAGE</u>
L	58	QB011		MH	4C	QB021
LA	41	QE001		MP	FC	QS041
LC	52	QQ101		MR	1C	QB021
LCDR	23	QC001		MVC	D2	QP001
LCER	33	QC001		MVI	92	QK001
LCR	13	QB011		MVN	D1	QP011
LD	68	QG011		MMVD	F1	QS121
LDR	28	QC001		MVW	D8	QQ071
LE	78	QG011		MVZ	D3	QP011
LER	38	QC001				
LH	48	QB011		N	54	QF001
LI	0C	QQ101		N	D4	QP021
				NI	94	QK001
LM	98	QK011		NK	14	QP021
LNDR	21	QC001				
LNER	31	QC001		O	56	QF001
LNR	11	QB011		OC	D6	QP021
LPDR	20	QC001		OI	96	QK001
LPER	30	QC001		OR	16	QP021
LPH	10	QB011				
LPSB	A1	QQ041		PACK	F2	QS101
LPSW	82	QJ031				
LR	18	QB011		RDD	85	QJ001
LTDH	22	QC001		RPSB	0F	QQ401
LTER	32	QC001				
LTR	12	QB011		S	5B	QF001
				SATR	0D	QQ021
M	5C	QB021		SCON	01	QQ001
MD	6C	QG011		SD	6B	QG001
MDH	2C	QC031		SDR	2B	QC061
ME	7C	QG011		SE	7B	QG001
MER	3C	QC031		SER	3B	QC061

CAS INDEX

<u>MNEMONIC</u>	<u>OP CODE</u>	<u>CAS PAGE</u>	<u>MNEMONIC</u>	<u>OP CODE</u>	<u>CAS PAGE</u>
SH	4B	QB001	TCR	9F	QK021
SIO	9C	QK021	TIO	9D	QK021
SIOP	9A	QK021	TM	91	QK001
SL	5F	QF001	TR	DC	QP051
SLA	8B	QJ504	TRT	DD	QP051
			TS	93	QK021
SLDA	8F	QJ021			
SLDL	8D	QJ021	JNPK	F3	QS111
SLL	89	QJ504			
SLR	1F	QB001	WRD	84	QJ041
SP	FB	QS001			
SPCI	9B	QK021	X	57	QF001
SPM	04	QJ031	XC	D7	QP021
SPSB	A0	QQ041	XI	97	QK001
SR	1B	QB001	XR	17	QP021
SRA	8A	QJ001			
SRDA	BE	QJ011	ZAP	F8	QS031
SRDL	8C	QJ011			
SRL	88	QJ001			
SSK	08	QJ031			
SSM	80	QJ031			
ST	50	QE001			
STC	42	QE001			
STD	60	QG001			
STE	70	QG001			
STH	40	QE001			
STM	90	QK011			
SU	7F	QG001			
SUR	3F	QC061			
SVC	0A	QJ031			
SW	6F	QG001			
SWR	2F	QC061			

CAS INDEX

<u>MISC ROS FUNCTIONS</u>	<u>CAS PAGE</u>		<u>MISC ROS FUNCTIONS</u>	<u>CAS PAGE</u>
DIAGNOSE KERNELS			INVALID OPS	
DEFINE STORAGE	QQ181		RR AND RX	QT051
LOG-OUT FAA	QQ041		RS AND SI	QT061
LOG-OUT LOCAL STORE	QQ181		IPL	QY061
LOG-OUT MAIN STORAGE	QQ171		LOG-OUT	QY001
LOG-OUT REGISTERS	QQ181		MANUAL OPERATIONS	
PARTIAL SCAN-IN	QY011		DISPLAY	QY041
RESET CHECKS	QQ171		IPL/PSW	QY061
SCAN-IN	QY011		LOAD REGISTER	QY041
SET DAR MASK	QQ181		MACHINE RESET	QY041
STORE DAR	QQ181		ROS TRANSFER	QY061
STORE PIR	QQ181		SET IC	QY051
WRAP	QQ171		START	QY041
FLT TEST			STOP	QY041
READ IN	QY011		STORE	QY041
SCAN IN	QY015,QY021		PULSE MODE	QY051
ERROR ROUTINE	QY031		PROGRAM STORE COMPARE	QT041
I FETCH			Q BUFFER REFILL	QT041
RR FORMAT	QT001		RECEIVE ATR	QQ031
RS OR SI FORMAT	QT005		REPEAT INSTRUCTION	QY051
RX FORMAT	QT011		RIPPLE	
SS FORMAT	QT021,QT031		READ	QY051
INTERRUPTS			WRITE	QY051
EXTERNAL	QU001		STOP LOOP	QY041
INPUT/OUTPUT	QU001		TIME CLOCK STEP	QT041
MACHINE CHECK	QU001		WAIT LOOP	QY051
PROGRAM	QU001			
SUPERVISOR CALL	QU001			

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CAS INDEX

FORCED ADDRESSES TO ROSAR

<u>PRIORITY</u>	<u>FUNCTION</u>	<u>FORCED ADDRESS</u>	<u>CAS PAGE</u>
6	EXTERNAL INTERRUPT	0006	QU001
12	INVALID INSTRUCTION ADDR	0002	QT041
7	I/O INTERRUPT	000E	QU001
3	MACHINE CHECK INTERRUPT	000C	QU001
	MACHINE RESET	0003	QY041
8	MANUAL CONTROL STOP	0026	QY041
	PAGING SPECIFICATION	0007	QU001
	POWER ON RESET	000B	QY041
4	PROGRAM INTERRUPT	000A	QU001
11	PROGRAM STORE COMPARE	0004	QT041
	PULSE MODE	0005	QY051
	Q REFILL RX FORMAT	0022	QT041
	Q REFILL RR FORMAT	0030	QT041
	Q REFILL RX FORMAT	0032	QT041
	Q REFILL RX FORMAT	003A	QT041
	Q REFILL RS-SI FORMAT	0024	QT041
	Q REFILL RS-SI FORMAT	0034	QT041
	REFILL SHIFT INSTRUCTION	0020	QJ001
10	REPEAT INSTRUCTION	0028	QY051
2	SAP INTERRUPT DELAY (CPU STORE IN PROGRESS)	002E	QU001
	SCAN-LOG-OUT	0019	QY001
	SCAN MCW4	0009	QY031
	SCAN MASK	0011	QY031
	SPECIFICATION	0010	QT041
5	SVC INTERRUPT	0008	QU001
1	TIME CLOCK STEP/ RECEIVE ATR/EXT. START	0014	QT041
9	WAIT STOP	002A	QY051

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MICRO-ORDER INDEX

<u>MICRO-ORDERS DEC ORDER</u>		<u>MICRO-ORDERS DEC ORDER</u>	
A	A11	BCNMΩ	J11
A	T8	BEOP	D3
AB	A5	BL2	T1
AB	T12	B38M	A7
ABC+1	F53	B489	T15
ABC-1	F49	B8	A13
ABC=0	J7	B8	T9
ABC=7	J39	B8J9	T7
ABC≠3	J65	B, IC	A2
ABC.STC+1	F52		
ABC.STC-1	F48	CONTIN	J67
ABL2	T5	CON→E3	E8
AB17	A4		
AB17	T14	D	C15
AB18	A14	DATA-KEYS→ST	C18
AB18	T14	DEC	K10
AB38	A6	DEC	T3
AB→U	R0	DEC DIV	J82
ADRSQNCR-1	SD2	DECIMAL	J98
ADR-KEYS→D	C11	DECOFLO→STAB	G6
ATL,MS-TEST	J124	DIR-CNTL→F	D4
ATRSELΔRESET	C16	DIS-PB	J25
A13	T10	DREG(18-23)	J96
A1=0,J5=0	J123	DT	C5
A1≠0→INH	F11	DTS	C24
A,B	A3	DVDLO	G20
A(07)=0→INH	F10	DVDL1	G21
		DVD-CHECK	F18
B	A1	DWS	C12
B	T11	D1→E3	E9

MICRO-ORDER INDEX

MICRO-ORDERS DEC ORDER

D22=1	J38
D2=3	J15
D(21)	K6
D→STC	F47
E	E3
EDIT	J104
EDIT-CTL	F60
EEOP	D2
EXCEP	K25
E2	V2
E23	V3
E23-1	E7
E23=0	K16
E2+1	E1
E2-1	E5
E2=E3	J33
E2=0/	K3
E2=15	K4
E2,3-1	E4
E3	V1
E3+1	E2
E3-1	E6
E3=0	K19
E3=0/	K20
E3=15	K2
E3=255	J48
E3≠1	J16
E3≠3	J17

MICRO-ORDERS DEC ORDER

E3≠4	J32
E3→ABC	F57
E3→ABC,STC	F56
E3→STC	F58
E=0/	K18
E(02-07)→ROA	J103
E(03)	J22
E(04-07)→ROA	J102
F	D7
FLPT-UN,COMP	J105
FLR	J120
FLT1	A6.U1
FLT2	A5.D7
	N7.M30
	RO.T12
	U5
FLT3	A5.D7
	N14.M28
	P5.RO
	T12.U15
FLT4	A5.D7
	M24.N2
	P2.RO
	T5,U7
FLTΔINITLIZE	SG10
FXPOFLO→STAB	G3
FO	D5
F1	D6
F1	T4
F1≠1	K22

MICRO-ORDER INDEX

<u>MICRO-ORDERS DEC ORDER</u>		<u>MICRO-ORDERS DEC ORDER</u>	
F1≠9	K23	J47≠0	K14
F→J	R1	J49B	A12
		J57=0	J9
G	C22	J7→ABC	F46
		J7→STC	F43
HLD△IN	J36	J9B8 ..	A8
HSMOVE	J26	J(58-63)	J122
IC	A10	LOGIC-COMP	J107
IC	T2	LS-PB	J5
IC3=3	J13	L→	P5
IC=PB	J31		
IC(21-22)	J99	MCW04	J19
IC→ABC	F14	MOVE	K27
IF-INV→TGR	F38	MPLY-END	F12
INH-MS-PROT	G25	MSK-ADR→SAB	SD5
INH-W-PAR-CK	F31	MS-REQ*D-3	L10
INSERT-KEY	G27	MS-REQ*D-4	L11
INTRP	K21	MS-REQ*IC-3	L8
INV-ADR→TGR	G24	MS-REQ*IC-4	L9
IPL△PSW	J30	MS-REQ*SCAN4	L13
		MSO→S	C29
JCRY28	J4	MSO→T	C10
JCRY4	J86	MS1→T	C8
JWT	C6	MS*IC-3*D=11	L12
J1=0,J17=0	J111	MS→AB	A9
J1=0/1,J17=0	J109	MS→Q	C20
J1=0/1,J18=0	J109	MS→ST	C9
J47=0	J10	MS→T*D(21)	C26
J47=0.OFLO	J8	M/DVD	J29
J47=1	J80		

MICRO-ORDER INDEX

<u>MICRO-ORDERS DEC ORDER</u>		<u>MICRO-ORDERS DEC ORDER</u>	
NEOP	D1	RG*Q0	H4
NEXT-INST*D	J121	RG*Q2	H5
NEXT-INST*IC	J97	RG*Q4	H6
		RG*Q6	H7
PSW39	K9	RG*R2	H25
PSW→ST	C1	ROS-PB	J85
PSW→S23	C2	RSLT-SIGN→LS	F40
		R*E11-15	H23
QUOT	N5	R*E3	H20
Q01→R	E12	R*24	H26
Q1	V7	R→	P2
Q23→R	E13	R→E	E10
Q3	V6	RΔATR1	H95
Q45→R	E14	RΔATR2	W8
Q5	V5	RΔCCR	H94
Q67→R	E15	RΔCKREG2	H85
Q7	V4	RΔDAR	H92
Q→R*D	G9	RΔDARMSK	H93
		RΔEXTBUS	W12
R	E11	RΔEXTREG	H65
RASCR	G15	RΔFP0	H48
RELI/O	J52	RΔFP1	H49
RESET	F1	RΔFP2	H50
RF*E2	H10	RΔFP3	H51
RF*E2Ω1	H8	RΔFP4	H52
RF*E3	H17	RΔFP5	H53
RF*E3Ω1	H16	RΔFP6	H54
RF*R2	H24	RΔFP7	H55
RG*E2	H14	RΔGP0	H32
RG*E2Ω1	H12	RΔGP1	H33
RG*E3Ω1	H18	RΔGP2	H34

<u>MICRO-ORDERS DEC ORDER</u>		<u>MICRO-ORDERS DEC ORDER</u>	
RΔGP3	H35	SEL-MPL*E3	G30
RΔGP4	H36	SET-CR	F63
RΔGP5	H37	SET-KEY	G26
RΔGP6	H38	SET-MARK-0-3	L5
RΔGP7	H39	SET-MARK-0-7	L4
RΔGP8	H40	SET-MARK*J61	L7
RΔGP9	H41	SET-MARK*STC	L6
RΔGP10	H42	SIGNS→STATS	F2
RΔGP11	H43	SPEC	K31
RΔGP12	H44	ST	C14
RΔGP13	H45	STAA	J81
RΔGP14	H46	STAB	J50
RΔGP15	H47	STAC→STAF	F36
RΔGREG	W11	STAD	K5
RΔPSBAR	H66	STAD, STAG	J108
RΔSELREG	H67	STAE	K11
		STAE, FISGN+	J101
SAJOS	F22	STAF=C	J84
SAMPLEΔVALUE	W4	STAG	K8
SASCR	F24	STAH	J66
SAS=0	J49		
SAS=2, 3, 4	J110	STC+1	F54
SAS=13	J53	STC-1	F50
SAVE-SIGNS	F6	STC=7	J23
SB-PB	J37	STC≠3	J55
SCANOUT-LTWD	SG4	STOP 1	L1
SCANOUT-RTWD	SG1	STOP 2	L2
SCANOUT-SREG	SD6	STOP.1→UNCND	SF4
SCANOUT-TREG	SF7	STO-PB	J21
SCAN-BYPASS	P1	STT-PB	J34
SCAN-IN	SG14	ST04→PSW	C3

SYS RESET thru 0

MICRO-ORDER INDEX

<u>MICRO-ORDERS DEC ORDER</u>		<u>MICRO-ORDERS DEC ORDER</u>	
SYSTEM-RESET	SG12	W=0	J68
SO→PSW	C28	W*E11-15	H19
		W*24	H27
T	C4	WΔFP0	H112
TCS/ST	J69	WΔFP1	H113
TEST-AND-SET	G31	WΔFP2	H114
TIF	C21	WΔFP3	H115
T4→PSW	C17	WΔFP4	H116
T,D	C7	WΔFP5	H117
T/T.T	J70	WΔFP6	H118
T(32)	J3	WΔFP7	H119
TB→ΔMCW	C19	WΔGP0	H96
T→RAR	K24	WΔGP1	H97
		WΔGP2	H98
UFLO	J28	WΔGP3	H99
UFMSK	K28	WΔGP4	H100
		WΔGP5	H101
V	N2	WΔGP6	H102
V0.V0	N14	WΔGP7	H103
V0.0	N10	WΔGP8	H104
V0,+	N4	WΔGP9	H105
V0.-	N12	WΔGP10	H106
		WΔGP11	H107
WCRY	K17	WΔGP12	H108
WF*E2	H11	WΔGP13	H109
WF*E2Q1	H9	WΔGP14	H110
WG*E2	H15	WΔGP15	H111
WG*E2Q1	H13		
W1=1	K15	XECTGR	J20
W1=15	K13		
W1=(01-15)	J100	0	J0
W-CRY	J2	0	K0

MICRO-ORDER INDEX

<u>MICRO-ORDERS</u>	<u>DEC</u>	<u>ORDER</u>	<u>MICRO-ORDERS</u>	<u>DEC</u>	<u>ORDER</u>
0		N0	1→MCH-CK-TRP		SF6
0		T0	1→OFLO/UFLO		F21
0		V0	1→PASS/FAIL		SG8
0,V		N6	1→SCAN-MODE		F41
0,V1		N3			
0→ABC		F15	1→STAA*J18=0		G2
0→ASC,XEC		F27	1→STAA*J47=0		F3
0→BR-INV-ADR		G23	1→STAA*W≠0		G1
0→IC(21-22)		G16	1→STAB,STAG		G7
0→INT-TGR		F25	1→STAB*J2632		G14
0→PASS/FAIL		SF8	1→STAB*J31=1		F39
0→SCAN-MODE		SG13	1→STAB*W=0		F5
0→STAA*J47≠0		F4	1→STAD		F9
0→STAD		F8	1→STAG		G8
0→STAG		F45	1→STAH		G13
0→STAH		G5	1→STC(00)		F59
0→STC		F51	1→STOP-LOOP		F7
0→STP,STPLP		F44	1→TCL-TGR		F17
0→TIC,GAP		SF5	1→TIME-GATE		F29
0→TIME-GATE		F30	1→XEC-TGR		F42
0→TIME-STEP		F28			
			2→IC(21-22)		G18
1		J1			
1		K1	3→IC(21-22)		G19
1		N15	3→STC		F55
1→ASC*J57=0		F26	3<STC		J71
1→CTRCTL-TGR		SF1			
1→IC(21-22)		G17	4<E3		J64
1→INST-MSREQ		G22			
1→INTREQ-TGR		F20	6<E23		K26
1→INV-OP-TGR		F19			

8 thru 8

MICRO-ORDER INDEX

MICRO-ORDERS DEC ORDER

8	T6
9,V1	N7
+D	U3
+DJ13	U11
+DT	U15
+DTL1	U7
+P	Q1
+S	U4
+T	U14
+TIME	Q5
+TL1	U6
+T45R	U8
+T67	U9
+U	M19
+U0,0	M17
+U1,U0	M13
+U1,0	M15
+0	M0
+0	U0
+0,U	M31
+0,U0	M29
+0,U1	M27
+1	Q3
+1,-U	M7
+15,U0	M21
+15,U1	M23
+6U	M24

MICRO-ORDERS DEC ORDER

+6U0,5	M26
+6U0,0	M25
+8	Q2
+ΔDECAB	M4
+ΔK	U16
+ΔT45R	U24
+ΔT67	U25
+Δ2	U20
+Δ32	U21
-D	U2
-DT	U12
-DTL1	U5
-D+7	U10
-T	U13
-TL1	U1
-U	M28
-U0,0	M30
-U,CRY	M5
-1	N11
-1	Q7
-8	Q6
-16	Q4
-64	N8
-ΔU	M7
,C8	P6
.U	M18
ΩU	M22
∇U	M20

MICRO-ORDER INDEX

<u>MICRO-ORDERS DEC ORDER</u>		<u>MICRO-ORDERS DEC ORDER</u>	
->	P0	▷ LOAD-REG	W9
-HOLD	P4	▷ MACH-RESET	SG12
-S	B1	▷ MS-REQ-LOG	L3
-S,T	B3	▷ MS-IM	W5
-T	B2	▷ NO-V	W10
		▷ N1	C31
▷ E3.RR	J24	▷ N1-V	W14
▷ F04	J14	▷ PIR-F	G29
▷ RR.C	K12	▷ RDD-T-0-CHK	F13
▷ STAC	J18	▷ REG-SET	J44
		▷ RQ-XY-STO*D	L14
?U*E1	M12	▷ RRS	K7
		▷ R1->	P7
▷ ABC-1,STC+1	F61	▷ SAS=18	J46
▷ ATRSEL	J27	▷ SE-DEF-F	G4
▷ CE-ID-F	G28	▷ STATE0	J43
▷ FLT	J35	▷ ST04-ATR	H31
▷ FMTN*E13-15	U18	▷ ST-V	E0
▷ FMTO*E13-15	U17	▷ TCS	J6
▷ FMTW*E14-15	U19	▷ TIC	J83
▷ GEN-BUS-PAR	W13	▷ T(63)	J40
▷ INVERT-BFR1	SG9	▷ T-DARMSK	H29
▷ IOCE	J41	▷ T-EXTREG	H1
▷ IOERR	J42	▷ T->M	W15
▷ J47≠0.	J125	▷ T-PSBAR	H2
▷ ↯CRY ▷ CRY		▷ T-SELREG	H3
▷ K	C30	▷ W(01-02)	J106
▷ IMT	J12	▷ 0001-V0	E17
▷ IMT1	W2	▷ 0010-V0	E18
▷ IMT2	W3	▷ 0011-V0	E19
▷ IM-N,Q-R*IC	C23	▷ 0100-V0	E20

thru ▷ 0100 ↑ V0

MICRO-ORDER INDEX

MICRO-ORDERS DEC ORDER

Δ 0101→V0	E21
Δ 0110→V0	E22
Δ 0111→V0	E23
Δ 0 → CC	F32
Δ 0→INTR-GATE	G11
Δ 1000→V0	E24
Δ 1001→V0	E25
Δ 1010→V0	E26
Δ 1011→V0	E27
Δ 1100→V0	E28
Δ 1101→V0	E29
Δ 1110→V0	E30
Δ 1111→V0	E31
Δ 1 → CC	F33
Δ 1→INTR-GATE	G10
Δ 1→IVSPEC	F16
Δ 2	T13
Δ 2 → CC	F34
Δ 3 → CC	F35
Δ 7→ADR-SQCR	SG11
Δ 13→ADR-SQCR	W1
Δ 15→ADR-SQCR	SD4
Δ 16→ADR-SQCR	SD3
Δ 23→ADR-SQCR	SG15
Δ 512CRY	J45
Δ 512CRY→DLT	F37
Δ 512CRY→ICLT	F23

CONTROL FIELDS AND MICRO-ORDERS

A FIELD INGATING TO A,B,IC

THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 06-09.

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
		0000	A0	NO OPERATION.	
A	B	0001	A1	PAL32-63 TO B32-63.	DR021
A	B,IC	0010	A2	PAL32-63 TO B32-63 AND PAL 40-63 TO IC00-23.	DR021
A	A,B	0011	A3	PAL32-63 TO BOTH A00-31 AND B32-63.	DR021,RY031
A	AB17	0100	A4	PAL 08-63 TO AB08-63 (DOES NOT RESET A00-07).	DR021
A	AB	0101	A5	PAL04-67 TO AB04-67 (RESETS A00-03).	DR021
A	AB38	0110	A6	PAL24-67 TO AB24-67.	DR021
A	B38M	0111	A7	PAL24-67 TO AB24-67 (PAL66,67 = 00, VALUE OF MULTIPLE SELECTION REGISTER (M1M2) TO PAL64,65).	DR021
A	J9B8	1000	A8	PAL28-31 TO B64-67 (PAL24-27 MUST = 0000 FOR CORRECT PARITY).	DR021
D	MS→AB	1001	A9	SDBO 00-63 TO AB00-63.	DR021
A	IC	1010	A10	PAL40-63 TO IC00-23.	DR021
A	A	1011	A11	PAL32-63 TO A00-31.	DR021
A	J49B	1100	A12	PAL32-63 TO B32-63, PAL28-31 TO B64-67 (PAL24-27 MUST = 0000 FOR CORRECT PARITY).	DR021
A	B8	1101	A13	PAL64-67 TO B64-67.	DR021
A	AB18	1110	A14	PAL08-67 TO AB08-67 (DOES NOT RESET A00-07).	

CONTROL FIELDS AND MICRO-ORDERS

B FIELD INGATING LOCAL STORE TO S,T

THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 10-11

EDGE CHAR	<u>MICRO-ORDER</u>	<u>BITS</u>	DEC <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
		00	B0	NO OPERATION.	DR021
L	-S	01	B1	LOCAL STORE DATA REG OUTPUT BUS00-31 TO S00-31.	DR021
L	-T	10	B2	LOCAL STORE DATA REG OUTPUT BUS00-31 TO T32-63.	DR021,RY031
L	-S,T	11	B3	LOCAL STORE DATA REG OUTPUT BUS00-31 TO BOTH S00-31 AND T32-63.	DR021

C FIELD REGISTER INGATING TO D,K,Q,S,T, PSW,N,G

THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 12-16

EDGE CHAR	<u>MICRO-ORDER</u>	<u>BITS</u>	DEC <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
		00000	C0	NO OPERATION.	
D	PSW→ST	00001	C1	PSW BITS TO S00-19, T32-39 (SYS MASK,KEY,AMWP,IILC,CC, PRG MASK), INTERRUPT RESET. (APPROPRIATE CODE TGR.) SDB000-63 TO Q00-63 (but if E 12-15= 0000 and RR or shift, then degate SDBO to Q)	DR031
D	PSW→S23	00010	C2	PSW BITS TO S20-31 (INTERRUPTION CODE).	DR041
D	ST04→PSW	00011	C3	S00-07 AND 16-19 TO PSW (SYSTEM MASK), S08-15 TO PSW (KEY,AMWP) T34-39 TO PSW (CC, PROG MASK).	DR031
A	T	00100	C4	PAL32-63 TO T32-63.	DR031
A	DT	00101	C5	PAL08-31 TO D00-23, PAL 32-63 TO T32-63.	DR031

CONTROL FIELDS AND MICRO-ORDERS

6

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
A	JWT	00110	C6	PAL40-63 TO T40-63 AND SAL00-07 TO T31-39 .	DR031
A	T,D	00111	C7	PAL32-63 TO T32-63, PAL40-63 TO D00-23 .	DR031
D	MS1→T	01000	C8	SDB032-63 TO T32-63 .	DR041
D	MS→ST	01001	C9	SDB000-63 TO ST00-63 .	DR041
D	M50→T	01010	C10	SDB000-31 TO T32-63 .	DR041
D	ARD-KEYS→D	01011	C11	ADDRESS KEYS TO D00-23 .	DR041
A	DWS	01100	C12	PAL40-63 TO D00-23, SAL00-07 TO ST PER STC .	DR031
B	ST	01110	C14	SAL00-07 TO ST PER STC .	DR031
A	D	01111	C15	PAL40-63 TO D00-23 .	DR031
C	ATRSEL ▽ RESET	10000	C16	RESET ATR SELECT LATCH .	DR031
D	T4→PSW	10001	C17	T34-39 TO PSW (CC,PROG MASK) .	DR031
D	DATA-KEYS →ST	10010	C18	DATA KEYS TO ST00-63 .	DR031
D	TB→▽MCW	10011	C19	T32-39,52 TO MAINTENANCE CONTROL WORD 0-7, 20, T53-57 TO ADR SEQ0-4, T58-61 TO FLT COUNTER 0-3, T62, 63 TO FLT CLOCK 0, 1 B TO EXTENDED MCW .	DR031
D	MS→Q	10100	C20	SDB000-63 TO Q00-63 .	DR031
A	TIF	10101	C21	(SDBO 00-63) TO Q00-63 AND TWO BYTES OF Q TO R PER D21,22. IF ROSAR 10=1, PAL 32-63 T33-63.63 RESET EXECUTE AND ADDR STORE COMP IF BXH OR BXLE AND ROSAR 10=1.	DR031
B	G	10110	C22	SAL00-07 TO G00-07 (DIRECT CONTROL).	DR031

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
D	△ LM-N, Q-R*IC	10111	C23	TWO BYTES OF IM TO N, AND TWO BYTES OF Q TO R PER IC 21-22.	DR031
A	DTS	11000	C24	PAL08-31 TO D00-23, PAL32-63 TO T32-63, SAL 00-07 TO ST PER STC.	DR021
D	MS→T*D(21)	11010	C26	SDB000-31 TO T32-63 IF D21=0, SDB032-63 TO T32-63 IF D21=1.	DR041
D	SO→PSW	11100	C28	S00-07, 16-19 TO PSW00-07, 16-19 (SYSTEM MASK).	DR031
D	MS0→S	11101	C29	SDB000-31 TO S00-31.	DR041
A	△ K	11110	C30	PAL 32-63 TO K 00-31.	DR041
B	△ N1	11111	C31	SAL 00-07 TO N 08-15.	DR031

D FIELD END OPS AND INGATING SERIAL ADDER TO F.
THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 17-19.

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
		000	DO	NO OPERATION.	
C	NEOP	001	D1	NORMAL END OP SET BLOCK I FETCH TGR IF EXCEPTIONAL CONDITION TO I FETCH. GATE INTERRUPT PRIORITY. IF R REGISTER OP IS NOT RR FORMAT, THEN GATE Q TO LAL PER IC21-22, IF RR and NOT BRANCH THEN GATE R8-11 TO LAL, OR IF RR AND BRANCH THEN GATE R12-15 to LAL. CHECK FOR Q-BUFFER REFILL AND START I FETCH SEQUENCERS IF THE BUFFER IS TO BE REFILLED.	DR051

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
C	EEOP	010	D2	EARLY END OP CHECK FOR Q-BUFFER REFILL AND START I FETCH SEQUENCERS IF THE BUFFER IS TO BE REFILLED.	DR051
C	BEOP	011	D3	BRANCH END OP SET BLOCK I FETCH TGR IF EXCEPTIONAL CONDITION TO I FETCH. GATE INTERRUPT PRIORITY. IF R REGISTER OP IS NOT RR FORMAT THEN GATE Q TO LAL PER D21-22, IF RR AND NOT BRANCH THEN GATE R8-11 TO LAL OR IF RR AND BRANCH THEN GATE R12-15 to LAL. CHECK FOR Q-BUFFER REFILL AND START I FETCH SEQUENCERS IF THE BUFFER IS TO BE REFILLED.	DR051
C	DIR- CNTL-F	100	D4	DIRECT CONTROL 00-07 TO F00-07.	DR051
B	F0	101	D5	SAL00-03 TO F00-03.	DR051
B	F1	110	D6	SAL04-07 TO F04-07.	DR051
B	F	111	D7	SAL00-07 TO F00-07.	DR051,RF901

CONTROL FIELDS AND MICRO-ORDERS

E FIELD INGATING TO E,R, E INCREMENTING AND DECREMENTING AND EMIT.
 THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 81,21-24 *

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
		* 81 21 24 ↓ ↓ ↓ 00000	E0	NO OPERATION.	
C	E2+1	00001	E1	E08-11 PLUS 1 TO E08-11.	DR051
C	E3+1	00010	E2	E12-15 PLUS 1 TO E12-15.	DR051
A	E	00011	E3	PAL 56-63 TO E08-15.	DR071
C	E2,3-1	00100	E4	E08-11 MINUS 1 TO E08-11, E12-15 MINUS 1 TO E12-15.	DR051,CE901
C	E2-1	00101	E5	E08-11 MINUS 1 TO E08-11.	DR051
C	E3-1	00110	E6	E12-15 MINUS 1 TO E12-15.	DR051
C	E23-1	00111	E7	E08-15 MINUS 1 TO E08-15.	DR051
D	CON→E3	01000	E8	CONSTANT TO E12-15 (5 IF FLTG. PT. DIVIDE, 15 IF FLTG. PT. OR FXD. PT. MULTIPLY, 0 IF OTHER).	DR051
D	D1→E3	01001	E9	D18-21 TO E12-15.	DR051
D	R→E	01010	E10	R00-15 TO E00-15 ALSO SETS ILC PER R00 and 01**.	DR071
A	R	01011	E11	PAL 56-63 TO R08-15.	DR071
D	Q01→R	01100	E12	Q00-15 TO R00-15.	DR071
D	Q23→R	01101	E13	Q16-31 TO R00-15.	DR071
D	Q45→R	01110	E14	Q32-47 TO R00-15.	DR071
D	Q67→R	01111	E15	Q48-63 TO R00-15.	DR071
B	∇NX→V	10000	E16	GATE N BYTE TO SBB-00-07 PER W10 OR W14 MICRO-ORDER.	XN231

**

	R00, 01	ILC
(RR)	0 0	01
(RX)	0 1	10
(RS, SI)	1 0	10
(SS)	1 1	11

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
B	0001-V0	10001	E17	GATE 0001 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	0010-V0	10010	E18	GATE 0010 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	0011-V0	10011	E19	GATE 0011 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	0100-V0	10100	E20	GATE 0100 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	0101-V0	10101	E21	GATE 0101 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	0110-V0	10110	E22	GATE 0110 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	0111-V0	10111	E23	GATE 0111 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	1000-V0	11000	E24	GATE 1000 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	1001-V0	11001	E25	GATE 1001 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	1010-V0	11010	E26	GATE 1010 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	1011-V0	11011	E27	GATE 1011 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	1100-V0	11100	E28	GATE 1100 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	1101-V0	11101	E29	GATE 1101 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	1110-V0	11110	E30	GATE 1110 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065
B	1111-V0	11111	E31	GATE 1111 TO SBB 00-03,ZEROES TO SBB 04-07.	RY065

*BIT 81 ON BLOCKS GATING A BYTE FROM ST TO SBB 00-07
REFERENCE ALD RT831, RT836.

CONTROL FIELDS AND MICRO-ORDERS

F FIELD MISC. CONTROL LINES ,

THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 25-30.

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
		000000	F0	NO OPERATION.	
C	RESET	000001	F1	*** I FETCH RESET *** RESET STAA THRU STAH. SET LALO IF FLOATING POINT OPS. E8-11 TO LAL ON RR BRANCH RESET STC AND ABC TO 000 (STC TO 100 ON RR FORMAT). RESET 3 CYCLE REQ TGR IF RS BRANCH. GATE FOR Q-BUFFER REFILL ON BRANCH INSTRUCTIONS.	DR101
C	SIGNS→STATS	000010	F2	SET STAT C IF NOT VFL DEC AND STO=1 -OR- VFL DEC AND SBA4-7 IS POSITIVE AND (COMP OR SUB) -OR- VFL DEC AND SBA4-7 IS NEGATIVE AND NOT (COMP OR SUB). SET STAT E IF VFL DEC AND INVALID SIGN. (BOTH OPERAND SIGNS ARE CHECKED). SET STAT F IF VFL DEC AND SBB SIGN IS NEGATIVE.	DR101
C	1→STAA*J47=0	000011	F3	SET STAA IF PAL 32-63=0.	
C	0→STAA*J47≠0	000100	F4	RESET STAA IF PAL32-63≠0 OR STAA LATCH=0.	
C	1→STAB*W=0 0	000101	F5	SET STAB IF SAL00-07=0.	
C	SAVE-SIGNS	000110	F6	SET STAT C IF FLPT AND (SUB OR COMP) AND SBB 0=0 -OR-	DR101

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
				FLPT AND NOT (SUB OR COMP) AND SBB0=1.	
				SET STAT D IF FLPT (MULT OR DIV) AND SALO=1.	
				SET STAT E IF NOT FLPT AND SBB4-7= INVALID SIGN.	
				SET STAT F IF FLPT AND ABO=1 OR NOT FLPT AND SBB IS NEGATIVE.	
C	1→STOP-LOOP	000111	F7	SET STOP LOOP (MANUAL) TRIGGER.	DR101
C	0→STAD	001000	F8	RESET STAD AND RESET BLOCK I FETCH TGR.	DR111
C	1→STAD	001001	F9	SET STAD.	DR111
C	A(07)=0→INH	001010	F10	INHIBIT INGATING FOR 1 CYCLE TO F,D,AB,ST,ROSAR IF A07 = 0.	DR111
C	A1≠0→INH	001011	F11	INHIBIT INGATING FOR 1 CYCLE TO F,D,AB,ST,ROSAR IF A08-11 DOES NOT = 0000.	DR111
C	MPLY-END	001100	F12	SELECTS MULTIPLIER BITS FROM S PER E12-15 AND TX TGR DURING TERMINAL CYCLE OF FIXED AND FLTG PT. MULTIPLY.	
C	△RDD-T-O-CHK	001101	F13	READ DIRECT TIME OUT INTERRUPT. TURN ON MACHINE CHECK AND PSW BIT 29.	DR125
D	IC→ABC	001110	F14	IC21-23 TO ABC INCR. LATCHES.	DR111
C	0→ABC	001111	F15	000 TO ABC INCR. LATCHES.	DR111
C	△1→IVSPEC	010000	F16	SETS SPECIFICATION INTERRUPT, PSW BITS 29, 30 UNCONDITIONAL IF 9020 OP.	DR091
C	1→TCL-TGR	010001	F17	SET TIME CLOCK AT LIMIT TGR.	DR091

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
C	DVD-CHECK	010010	F18	SET PROGRAM INTERRUPT TGRS PER SIGNIFICANCE OR DIVIDE CHK. CONDITIONS.	DR091
C	1→INV-OP-TGR	010011	F19	SET PROGRAM INTERRUPT TGR 1 (INVALID OP).	DR091
C	1→INTREQ-TGR	010100	F20	SET SUPERVISOR CALL TGR AND PROG. INTERRUPT TGRS IF SUPERVISOR CALL.	DR091
C	1→ OFLO/UFLO	010101	F21	SET PROGRAM INTERRUPT TGRS PER FLTG.PT. OR DECIMAL OVERFLOW OR UNDERFLOW CONDITIONS.	DR091
C	SAJOS	010110	F22	SET STAA IF E06 = 1 AND PAL 32-63 = 0, GATE RESULT SIGN ONTO LOCAL STORE BUS (T32 = 1 IF RESULT SIGN MINUS, =0 IF RESULT SIGN PLUS).	DR091
C	△ 512CRY→ICLT	010111	F23	SET IC CARRY LATCH IF PADDER 512 CARRY.	DR125
C	SASCR	011000	F24	SET ADDR. STORE COMP TGR IF PAL 32 CARRY.	DR121
C	0→INT-TGR	011001	F25	RESET MACH. CHK SUPV. CALL INTERRUPT TGRS INTERRUPT PRIORITY TGRS. SET STOP TGR IF INSTR. STEP.	DR121
C	1→ASC*J57=0	011010	F26	SET ADDRESS STORE COMPARE TGR IF PAL 40-63 = 0 OR IC21, 22 = 11 AND PAL 40-62 = 0.	DR121
C	0→ASC,XEC	011011	F27	RESET ADDR. STORE COMPARE AND EXECUTE TGRS.	DR121
C	0→TIME-STEP	011100	F28	RESET TIME CLOCK STEP TGR, CONDITION SET OF PULSE MODE ADJUST TGR.	DR121
C	1→TIME-GATE	011101	F29	SET TIMING GATE TGR.	DR121

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
C	0-TIME-GATE	011110	F30	RESET TIMING GATE TGR	DR121
C	INH-W-PAR-CK	011111	F31	INHIBIT SERIAL ADDER PARITY CHECK.	DR121
C	Δ0-CC	100000	F32	SET CONDITION CODE TO ZERO.	DR125
C	Δ1-CC	100001	F33	SET CONDITION CODE TO ONE.	DR125
C	Δ2-CC	100010	F34	SET CONDITION CODE TO TWO.	DR125
C	Δ3-CC	100011	F35	SET CONDITION CODE TO THREE.	DR125
C	STAC→STA F	100100	F36	SET STA TO STATE OF STAC.	DR121
C	Δ512CRY→DLT	100101	F37	SET D CARRY LATCH IF Padder 512 CARRY.	DR125
C	IF-INV-TGR	100110	F38	IF NOT 1→INST-MSREQ (G22 MICRO-ORDER) OR UNSUCCESSFUL BRANCH ON CONDITION AND IC21-22≠0 THEN SET GATE I FETCH ADDR TGR AND RESET I FETCH INVALID ADDR TGR AND INVALID INSTRUCTION ADDR TGR.	DR121
C	1→STAB*J31=1	100111	F39	SET STAB IF PAL 31=1	DR121
C	RSLT-SIGN→LS	101000	F40	GATE RESULT SIGN ONTO LOCAL STORE BUS (T32 = 1 IF RESULT SIGN MINUS, = 0 IF RESULT SIGN PLUS).	DR121
C	1→SCAN-MODE	101001	F41	SET SCAN MODE TGR.	DR091
C	1→XEC-TGR	101010	F42	SET EXECUTE TGR AND MAKE STORE REQ. (4 CYC) PER D IF SS FORMAT AND D21-22 = 10.	DR091
D	J7→STC	101011	F43	PAL61-63 TO STC	DR091
C	0→STP, STPLP	101100	F44	RESET STOP, STOP LOOP (MANUAL), AND PULSE MODE ADJUST TGRS, BLOCK INTERRUPTS ON START IF NOT WAIT STATE.	DR091
C	0→STAG	101101	F45	RESET STAG.	DR091

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
D	J7→ABC	101110	F46	PAL61-63 TO ABC.	DR091
D	D→STC	101111	F47	D21-23 TO STC INCR. LATCHES.	DR091
C	ABC,STC-1	110000	F48	ABC-1 TO ABC INCR. LATCHES AND STC-1 TO STC INCR. LATCHES.	DR101
C	ABC-1	110001	F49	ABC-1 TO ABC INCR. LATCHES.	DR101
C	STC-1	110010	F50	STC-1 TO STC INCR. LATCHES.	DR101
C	0→STC	110011	F51	SET STC. INCR. LATCHES TO 000.	DR101
C	ABC,STC+1	110100	F52	ABC PLUS 1 TO ABC INCR. LATCHES AND STC PLUS 1 TO STC INCR. LATCHES.	DR101
C	ABC+1	110101	F53	ABC PLUS 1 TO ABC INCR. LATCHES.	DR101
C	STC+1	110110	F54	STC PLUS 1 TO STC INCR. LATCHES.	DR101
C	3→STC	110111	F55	011 TO STC INCR. LATCHES.	DR101
D	E3→ABC,STC	111000	F56	E13-15 TO ABC INCR. LATCHES AND STC INCR. LATCHES.	DR111
D	E3→ABC	111001	F57	E13-15 TO ABC INCR. LATCHES.	DR111
D	E3→STC	111010	F58	E13-15 TO STC INCR. LATCHES.	DR111
C	1→STC(00)	111011	F59	FORCE 1 TO STC INCR. LATCH 0.	DR111
C	EDIT-CTL	111100	F60	IF STAG = 1, CONDITION EDIT HARDWARE CONTROLS.	DR111
C	∇ABC-1,STC+1	111101	F61	ABC-1 TO ABC INCR. LATCHES AND STC+1 TO STC INCR. LATCHES.	DR125
C	SET-CR	111111	F63	SET CONDITION CODE 01 IF	DR121

1) TM AND STAA *MIXED*

2) NOT STAA AND RESULT NEGATIVE
AND (NOT LOGICAL INSTR AND
NOT FXPT COMPARE AND FXPT OR
SHIFT ARITH)
LESS THAN ZERO

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
				3) (TRANSLATE OR EDIT) AND STAA AND (EO6 AND S TGR OR NOT EO6 AND NOT STAG) *TRT INCOMPLETE* *EDIT LESS THAN 0*.	
				4) FLPT AND NOT STAA AND RESULT SIGN MINUS *LESS THAN 0*.	
				5) DEC COMPARE AND(STA(A AND F AND H) OR STA(C AND F AND H) OR STA(A AND C AND NOT H)). *FIRST OP IS LOW*.	
				6) (DEC ADD OR DEC SUB OR ZERO AND ADD) AND STA(A AND H) *LESS THAN ZERO*.	
				7) ((AND) OR (OR) OR (EXCLUSIVE OR)) AND STAA *NOT 0*.	
				8) LOGICAL COMPARE(SI OR SS) AND STA(A AND NOT H) *1ST LOW*.	
				9) TEST AND SET AND ST32 *LEFT BIT IS ONE*.	
				10) ADD OR SUB LOG AND NOT STAA AND NOT AB31 *≠0, NO CARRY*.	
				11) FXPT COMP AND NOT STA(A AND B) AND ST32 OR FXPT COMP AND STA(NOT A AND B) AND NOT ST32 *1ST LOW*.	
				12) SIO OR TIO *CSW STORED*.	
				13) HIO *HALTED*.	
				14) TCH *CSW READY*.	

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
				SET CONDITION CODE 10 IF	
				1) TM AND STA(A AND H) *BITS ALL ONES*.	
				2) NOT STAA AND RESULT POS AND (NOT LOG INSTR AND NOT FXPT COMP AND FXPT OR SHIFT ARITH) *GREATER THAN ZERO*.	
				3) (TRANSLATE OR EDIT) AND STAA AND ((NOT S TGR AND E06) OR (STAG AND NOT E06) *TRT COMPLT* *EDIT GREATER THAN 0*.	
				4) FLPT AND NOT STAA AND RESULT POS *GREATER THAN 0*.	
				5) DEC COMP AND (STA(A AND NOT F AND H) OR STA(A AND NOT C AND NOT H) .	
				6) (DEC ADD OR DEC SUB OR ZERO AND ADD) AND STA(A AND NOT F) *GREATER THAN 0*.	
				7) LOG COMP (SI OR SS) AND STA (A AND H) *FIRST HIGH*.	
				8) LOG COMP (RR OR RX) AND NOT STAA AND AB31 *FIRST HIGH*.	
				9) (ADD OR SUB) LOG AND STAA AND AB31 *EQUAL 0, CARRY*.	
				10) FXPT COMP AND NOT STAA AND ((STAB AND ST32) OR (NOT STAB AND NOT ST32)) *FIRST HIGH*.	
				11) SIO *BUSY*.	
				12) HIO *STOPPED*.	
				13) TIO OR TCH *WORKING*.	

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
				SET CONDITION CODE 01 AND 10 IF	
				1) (FXPT AND NOT FXPT COMP OR ARITH SHIFT) AND STAB *OVERFLOW*.	
				2) DEC (ADD OR SUB) OR ZERO AND ADD AND STAB *OVERFLOW*.	
				3) (ADD OR SUB) LOG AND AB31 AND NOT STAA *≠0, CARRY*.	
				4) FLOATING POINT OVERFLOW.	

CONTROL FIELDS AND MICRO-ORDERS

G FIELD MISC. CONTROL LINES AND SET IC .

THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 31-35.

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
		00000	G0	NO OPERATION.	
C	1→STAA*W≠0	00001	G1	SET STAA IF SAL 00-07 DOES NOT = 0.	DR141
C	1→STAA*J18=0	00010	G2	SET STAA IF PAL 07-67 = 0.	DR141
C	FXPOFLO→STAB	00011	G3	SET STAB IF FIXED PT OVERFLOW (BLOCKS RESET OF STAB DURING PROGRAM INTERRUPT).	DR141
D	△ SE-DEF→F	00100	G4	GATE SE DEFINATION TO F 00-07.	DR151
C	0→STAH	00101	G5	RESET STAH (SERIAL ADDER CARRY TGR).	DR141
C	DECOFLO→STAB	00110	G6	SET STAB IF DECIMAL OVERFLOW (RESETS STAD).	DR141
C	1→STAB,STAG	00111	G7	SET STAB IF B32=1 AND STAG IF T32=1.	DR141
C	1→STAG	01000	G8	SET STAG.	DR131
D	Q→R*D	01001	G9	TWO BYTES OF Q TO R PER D21-22.	DR131
C	△ 1→INTR-GATE	01010	G10	SET INTERRUPT GATE TGR.	DR151
C	△ 0→INTR-GATE	01011	G11	RESET INTERRUPT GATE TGR.	DR151
C	1→STAH	01101	G13	SET STAH (SERIAL ADDER CARRY TGR).	DR131
C	1→STAB*J2632	01110	G14	SET STAB IF LEFT SHIFT OVERFLOW (BLOCKS RESET OF STAB DURING PROGRAM INTERRUPT).	DR131
C	RASCR	01111	G15	RESET ADDR. STORE COMP. TGR IF SUM 32 CARRY AND (PAL 40-63 DOES NOT=0 AND IC 21,22 DOES NOT = 11 OR PAL 40-62 DOES NOT =0) AND IC 21,22 = 11 AND EXECUTE NOT IN PROGRESS.	DR131

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
C	0→IC(21-22)	10000	G16	SET IC 21-22 TO 00.	DR141,DR191
C	1→IC(21-22)	10001	G17	SET IC 21-22 TO 01.	DR141,DR191
C	2→IC(21-22)	10010	G18	SET IC 21-22 TO 10.	DR141,DR191
C	3→IC(21-22)	10011	G19	SET IC 21-22 TO 11.	DR141,DR191
C	DVDLO	10100	G20	QUOTIENT BIT TO ODD SERIAL ADDER LATCH BIT PER E12-15. D,T TO PA PER MULTIPLE SELECT.	DR131 DR141
C	DVDL1	10101	G21	QUOTIENT BIT TO EVEN SERIAL ADDER LATCH BIT PER E12-15. D,T TO PA PER MULTIPLE SELECT.	DR131 DR141
C	1→INST-MSREQ	10110	G22	TURN ON INSTRUCTION MEMORY FETCH TGR.	DR131
C	0→BR-INV-ADR	10111	G23	RESET INVALID BRANCH AND INSTR ADDRESS TGRS.	DR131
C	INV-ADR→TGR	11000	G24	SET COND. CODE IF BRANCH INVALID ADDRESS TGR IS ON IN SS FORMAT (NOT EDIT AND NOT DEC. COMPARE OR E08-11=15.	DR131
C	INH-MS-PROT	11001	G25	TURN ON INHIBIT STORAGE PROTECT TGR.	DR141
C	SET-KEY	11010	G26	TURN ON SET KEY TGR. SET STAD.	DR141
C	INSERT-KEY	11011	G27	TURN ON INSERT KEY TGR. KEY 00-03 TO F 00-03. SET STAD.	DR141
D	∇ CE-ID→F	11100	G28	GATE CE IDENTITY BITS TO F 06-07. ZEROES TO F 00-05.	DR151
D	∇ PIR→F	11101	G29	GATE PROGRAM INTERRUPT REG. TO F 04-06. ZEROES TO F 00-03,07.	DR151

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
C	SEL-MPL*E3	11110	G30	SELECTS MULTIPLIER BITS FROM S PER E12-15 AND TX TGR (FIXED AND FLTG.PT. MULTIPLY.	DR141
C	TEST-AND-SET	11111	G31	STORAGE REQUEST PER D. STORE ALL ONES IN BYTE WITH MARK SET.	DR131

CONTROL FIELDS AND MICRO-ORDERS

H FIELD LOCAL STORE, FAA REGS, READ/WRITE CONTROLS AND ADDRESSING .
THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 36-42.

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<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
		0000000	H0	NO OPERATION.	
D	▷T-EXTREG	0000001	H1	GATE T 32-63 TO EXTERNAL REG.	DR171
D	▷T-PSBAR	0000010	H2	GATE T 32-63 TO PSBAR.	DR171
D	▷T-SELREG	0000011	H3	GATE T 32-63 TO SELECT REG.	DR171
L	RG*Q0	0000100	H4	READ GEN PURPOSE PER Q00-03, SET STAD IF Q00-03=0.	DR171
L	RG*Q2	0000101	H5	READ GEN PURPOSE PER Q16-19, SET STAD IF Q16-19=0.	DR171
L	RG*Q4	0000110	H6	READ GEN PURPOSE PER Q32-35, SET STAD IF Q32-35=0.	DR171
L	RG*Q6	0000111	H7	READ GEN PURPOSE PER Q48-51, SET STAD IF Q48-51=0.	DR171
L	RF*E2Ω1	0001000	H8	READ FLOATING PT. PER E08-11 (LAR04=1 OR E11).	DR161
L	WF*E2Ω1	0001001	H9	WRITE FLOATING PT. PER E08-11 (LAR04=1 OR E11) (FOR MULT. OR NOT SING. PREC.).	DR161,DR171
L	RF*E2	0001010	H10	READ FLOATING PT. PER E08-11.	DR161
L	WF*E2	0001011	H11	WRITE FLOATING PT. PER E08-11.	DR161,DR171
L	RG*E2Ω1	0001100	H12	READ GEN PURPOSE PER E08-11 (LAR04=1 OR E11).	DR161
L	WG*E2Ω1	0001101	H13	WRITE GEN PURPOSE PER E08-11 (LAR04=1 OR E11).	DR161,DR171
L	RG*E2	0001110	H14	READ GEN PURPOSE PER E08-11.	DR161

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
L	WG*E2	0001111	H15	WRITE GEN PURPOSE PER E08-11.	DR161,DR171
L	RF*E3Ω1	0010000	H16	READ FLOATING PT. PER E12-15 (LAR04=1 OR E15).	DR161
L	RF*E3	0010001	H17	READ FLOATING PT. PER E12-15.	DR161
L	RG*E3Ω1	0010010	H18	READ GEN PURPOSE PER E12-15 (LAR04=1 OR E15).	DR161
L	W*E11-15	0010011	H19	WRITE PER E11-15 (STORE-MANUAL CONTROLS).	DR161,DR171
L	R*E3	0010100	H20	READ GEN PURPOSE PER E12-15.	DR161
L	R*E11-15	0010111	H23	READ PER E11-15 (DISPLAY-MANUAL CONTROLS).	DR161
L	RF*R2	0011000	H24	READ FLOATING PT. PER R08-11.	DR161
L	RG*R2	0011001	H25	READ GEN PURPOSE PER R08-11.	DR161
L	R*24	0011010	H26	READ WORKING REGISTER (REG 24).	DR161
L	W*24	0011011	H27	WRITE WORKING REGISTER (REG 24).	DR171
D	ΔT→DARMSK	0011101	H29	GATE T32-63 TO DAR MASK REGISTER.	DR161
D	ΔST04→ATR	0011111	H31	GATE ST00-39 TO ADDRESS TRANSLATION REGISTER.	DR161
L	RΔGP0	0100000	H32	READ GEN PURPOSE REGISTER 0.	DR171
L	RΔGP1	0100001	H33	READ GEN PURPOSE REGISTER 1.	DR171
L	RΔGR2	0100010	H34	READ GEN PURPOSE REGISTER 2.	DR171
L	RΔGP3	0100011	H35	READ GEN PURPOSE REGISTER 3.	DR171

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
L	RΔGP4	0100100	H36	READ GEN PURPOSE REGISTER 4.	DR171
L	RΔGP5	0100101	H37	READ GEN PURPOSE REGISTER 5.	DR171
L	RΔGP6	0100110	H38	READ GEN PURPOSE REGISTER 6.	DR171
L	RΔGP7	0100111	H39	READ GEN PURPOSE REGISTER 7.	DR171
L	RΔGP8	0101000	H40	READ GEN PURPOSE REGISTER 8.	DR171
L	RΔGP9	0101001	H41	READ GEN PURPOSE REGISTER 9.	DR171
L	RΔGP10	0101010	H42	READ GEN PURPOSE REGISTER 10.	DR171
L	RΔGP11	0101011	H43	READ GEN PURPOSE REGISTER 11.	DR171
L	RΔGP12	0101100	H44	READ GEN PURPOSE REGISTER 12.	DR171
L	RΔGP13	0101101	H45	READ GEN PURPOSE REGISTER 13.	DR171
L	RΔGP14	0101110	H46	READ GEN PURPOSE REGISTER 14.	DR171
L	RΔGP15	0101111	H47	READ GEN PURPOSE REGISTER 15.	DR171
L	RΔFP0	0110000	H48	READ FLOATING PT. REGISTER 0.	DR171
L	RΔFP1	0110001	H49	READ FLOATING PT. REGISTER 1.	DR171
L	RΔFP2	0110010	H50	READ FLOATING PT. REGISTER 2.	DR171
L	RΔFP3	0110011	H51	READ FLOATING PT. REGISTER 3.	DR171
L	RΔFP4	0110100	H52	READ FLOATING PT. REGISTER 4.	DR171
L	RΔFP5	0110101	H53	READ FLOATING PT. REGISTER 5.	DR171
L	RΔFP6	0110110	H54	READ FLOATING PT. REGISTER 6.	DR171
L	RΔFP7	0110111	H55	READ FLOATING PT. REGISTER 7.	DR171
		1000000	H64	BLOCK GEN PURPOSE REG 0 AND GATE 9020 REG SELECTED BY W FIELD TO LOCAL STORE BUSS.	RY131
L	RΔEXTREG	1000001	H65	BLOCK GEN PURPOSE REG 0 AND GATE EXTERNAL REG TO L.S. BUSS.	DR171

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
L	RΔPSBAR	1000010	H66	BLOCK GEN PURPOSE REG 0 AND GATE LOGICAL PSBAR TO L.S. BUSS 9-19; PHYSICAL PSBAR TO L.S. BUSS 28-31.	DR171
L	RΔSELREG	1000011	H67	BLOCK GEN PURPOSE REG 0 AND GATE SELECT REG TO L.S. BUSS.	DR171
L	RΔCKREG2	1010101	H85	BLOCK GEN PURPOSE REG 0 AND GATE CHECK REG 2 TO L.S. BUSS.	DR161
L	RΔDAR	1011100	H92	BLOCK GEN PURPOSE REG 0 AND GATE DAR TO L.S. BUSS.	DR161
L	RΔDARMSK	1011101	H93	BLOCK GEN PURPOSE REG 0 AND GATE DAR MASK TO L.S. BUSS.	DR161
L	RΔCCR	1011110	H94	BLOCK GEN PURPOSE REG 0 AND GATE CONFIGURATION CONTROL REG TO L.S. BUSS.	DR161
L	RΔATR1	1011111	H95	BLOCK GEN PURPOSE REG 0 AND GATE ADDRESS TRANSLATION REG SECTION 1 TO L.S. BUSS.	DR161
L	WΔGPO	1100000	H96	WRITE GEN PURPOSE REGISTER 0.	DR171
L	WΔGP1	1100001	H97	WRITE GEN PURPOSE REGISTER 1.	DR171
L	WΔGP2	1100010	H98	WRITE GEN PURPOSE REGISTER 2.	DR171
L	WΔGP3	1100011	H99	WRITE GEN PURPOSE REGISTER 3.	DR171
L	WΔGP4	1100100	H100	WRITE GEN PURPOSE REGISTER 4.	DR171
L	WΔGP5	1100101	H101	WRITE GEN PURPOSE REGISTER 5.	DR171
L	WΔGP6	1100110	H102	WRITE GEN PURPOSE REGISTER 6.	DR171
L	WΔGP7	1100111	H103	WRITE GEN PURPOSE REGISTER 7.	DR171
L	WΔGP8	1101000	H104	WRITE GEN PURPOSE REGISTER 8.	DR171
L	WΔGP9	1101001	H105	WRITE GEN PURPOSE REGISTER 9.	DR171
L	WΔGP10	1101010	H106	WRITE GEN PURPOSE REGISTER 10.	DR171

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
L	WΔGP11	1101011	H107	WRITE GEN PURPOSE REGISTER 11.	DR171
L	WΔGP12	1101100	H108	WRITE GEN PURPOSE REGISTER 12.	DR171
L	WΔGP13	1101101	H109	WRITE GEN PURPOSE REGISTER 13.	DR171
L	WΔGP14	1101110	H110	WRITE GEN PURPOSE REGISTER 14.	DR171
L	WΔGP15	1101111	H111	WRITE GEN PURPOSE REGISTER 15.	DR171
L	WΔFP0	1110000	H112	WRITE FLOATING PT. REGISTER 0.	DR171
L	WΔFP1	1110001	H113	WRITE FLOATING PT. REGISTER 1.	DR171
L	WΔFP2	1110010	H114	WRITE FLOATING PT. REGISTER 2.	DR171
L	WΔFP3	1110011	H115	WRITE FLOATING PT. REGISTER 3.	DR171
L	WΔFP4	1110100	H116	WRITE FLOATING PT. REGISTER 4.	DR171
L	WΔFP5	1110101	H117	WRITE FLOATING PT. REGISTER 5.	DR171
L	WΔFP6	1110110	H118	WRITE FLOATING PT. REGISTER 6.	DR171
L	WΔFP7	1110111	H119	WRITE FLOATING PT. REGISTER 7.	DR171

CONTROL FIELDS AND MICRO-ORDERS

J FIELD CONDITIONAL BRANCHES (ROSAR BIT 11) AND FUNCTIONAL BRANCHES,
THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 62-68.

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
R	0	0000000	J0	RESET ROSAR 11 (UNCONDITIONAL).	
R	1	0000001	J1	SET ROSAR 11 (UNCONDITIONAL).	DS111
R	W-CRY	0000010	J2	SET ROSAR 11 IF CARRY OUT OF SERIAL ADDER (STAH NOT USED).	DS111
R	T(32)	0000011	J3	SET ROSAR 11 IF T32=1.	DS111
R	JCRY28	0000100	J4	SET ROSAR 11 IF PAL 28 CARRY = 0.	DS111
R	LS-PB	0000101	J5	SET ROSAR 11 IF LOCAL STORE PUSHBUTTON ON.	DS122
R	ΔTCS	0000110	J6	SET ROSAR 11 IF TIME CLOCK STEP.	DS151
R	ABC=0	0000111	J7	SET ROSAR 11 IF ABC = 000.	DS111
R	J47=0.OFLO	0001000	J8	SET ROSAR 11 IF PAL63=0 AND (STAG AND F4-7=POS OR NOT STAG AND F4-7=NEG.	DS161
R	J57=0	0001001	J9	SET ROSAR 11 IF PAL 40-64=0 (FOR WORD OVERLAP TEST).	DS111
R	J47=0	0001010	J10	SET ROSAR 11 IF PAL32-63=0.	DS111
R	BCNMΩ	0001011	J11	SET ROSAR 11 IF CONDITION NOT MET FOR BRANCH ON CONDITION OR IF RR FORMAT AND E12-15=0.	DS141
R	ΔLMT	0001100	J12	SET ROSAR 11 IF LIMIT LATCH IS ON.	DS151
R	IC3=3	0001101	J13	SET ROSAR 11 IF IC21-22=11.	DS113
R	γF04.	0001110	J14	SET ROSAR 11 IF F04=0 AND PAL CARRY 32=1.	DS113

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
R	D2=3	0001111	J15	SET ROSAR 11 IF D21-22=11.	DS141
R	E3≠1	0010000	J16	SET ROSAR 11 IF E12-15 DOES NOT = 0001.	DS141
R	E3≠3	0010001	J17	SET ROSAR 11 IF E14-15 DOES NOT = 11.	DS121
R	¬STAC	0010010	J18	SET ROSAR 11 IF STAC = 0.	DS113
R	MCW04	0010011	J19	SET ROSAR 11 IF MAINTENANCE CONTROL WORD 04=1.	DS131
R	XECTGR	0010100	J20	SET ROSAR 11 IF EXECUTE TGR = 1.	DS131
R	STO-PB	0010101	J21	SET ROSAR 11 IF STORE PUSHBUTTON ON.	DS122
R	E(03)	0010110	J22	SET ROSAR 11 IF E03=1.	DS141
R	STC=7	0010111	J23	SET ROSAR 11 IF STC=111.	DS121
R	¬E3.RR	0011000	J24	SET ROSAR 11 IF RR FORMAT AND E12-15 = 0000.	DS141
R	DIS-PB	0011001	J25	SET ROSAR 11 IF DISPLAY PUSHBUTTON ON.	DS122
R	HSMOVE	0011010	J26	SET ROSAR 11 IF E08-15 GREATER THAN 6 AND BOTH ABC AND STC=000.	DS121
R	Δ ATRSEL	0011011	J27	SET ROSAR 11 IF RECEIVE ATR SELECT IS ON.	DS171 DS105
R	UFLO	0011100	J28	SET ROSAR 11 IF SALO=1 AND INGATING NOT INHIBITED OR FO=1 AND INGATING INHIBITED (UNDERFLOW).	DS151
R	M/DVD	0011101	J29	SET ROSAR 11 IF DECIMAL MULTIPLY OR DIVIDE.	DS131

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
R	IPL Δ PSW	00i11110	J30	SET ROSAR 11 AFTER FALL OF 2500 MICRO-SECONDS S.S. IF IPL OR PSW RESTART PUSHBUTTON HAS BEEN DEPRESSED.	DS151
R	IC-PB	00111111	J31	SET ROSAR 11 IF SET INSTR. COUNTER PUSHBUTTON ON.	DS122
R	E3 \neq 4	01000000	J32	SET ROSAR 11 IF E12-15 DOES NOT = 100.	DS141
R	E2=E3	01000001	J33	SET ROSAR 11 IF E08-11 = E12-15.	DS121
R	STT-PB	0100010	J34	SET ROSAR 11 IF START PUSHBUTTON ON.	DS122
R	Δ FLT	0100011	J35	SET ROSAR 11 IF FLT MODE.	DS131
R	HLD Δ IN	0100100	J36	SET ROSAR 11 IF HOLD I/O LINE (DIRECT CONTROL).	DS151
R	SB-PB	0100101	J37	SET ROSAR 11 IF MAIN STORE BYTE PUSHBUTTON ON.	DS151
R	D22=1	0100110	J38	SET ROSAR 11 IF D22=1.	DS141
R	ABC=7	0100111	J39	SET ROSAR 11 IF ABC=111.	DS121
R	Δ T(63)	0101000	J40	SET ROSAR 11 IF T REG BIT 63=1.	DS171
R	Δ IOCE	0101001	J41	SET ROSAR 11 IF IOCE OPERATION.	DS171
R	Δ IOERR	0101010	J42	SET ROSAR 11 IF IOCE ERROR.	DS171
R	Δ STATE0	0101011	J43	SET ROSAR 11 IF IN STATE 0.	DS171
R	Δ REG-SET	0101100	J44	SET ROSAR 11 IF REGISTER SET PUSHBUTTON ON.	DS171
R	Δ 512CRY	0101101	J45	SET ROSAR 11 IF CARRY INTO PAL 54.	DS111

CONTROL FIELDS AND MICRO-ORDERS

EDGE CHAR	MICRO-ORDER	BITS	DEC ORDER	FUNCTION	ALD
R	Δ SAS=18	0101110	J46	SET ROSAR 11 IF SCAN ADDRESS SEQUENCER = 18.	DS151
R	E3=255	0110000	J48	SET ROSAR 11 IF E08-15 = 1111 1111.	DS141
R	SAS=0	0110001	J49	SET ROSAR 11 IF SCAN ADDRESS SEQUENCER = 0.	DS122
R	STAB	0110010	J50	SET ROSAR 11 IF STAB = 1.	DS131
R	RELI/O	0110100	J52	SET ROSAR 11 IF RELEASE I/O LINE (DIRECT CONTROL).	DS151
R	SAS=13	0110101	J53	SET ROSAR 11 IF SCAN ADDRESS SEQUENCER = 13.	DS122
R	STC≠3	0110111	J55	SET ROSAR 11 IF STC DOES NOT = 011.	DS121
R	4<E3	1000000	J64	SET ROSAR 11 IF E12-13 DOES NOT = 00.	DS141
R	ABC≠3	1000001	J65	SET ROSAR 11 IF ABC DOES NOT = 011.	DS121
R	STAH	1000010	J66	SET ROSAR 11 IF STAH=1 (SERIAL ADDER CARRY).	DS131
R	CONTIN	1000011	J67	SET ROSAR 11 IF ONE OF THE FOLLOWING CONDITIONS IS MET.	

MCW 5	MCW 6	PASS TGR	FAIL TGR
0	0	X	1
0	X	1	0

R	W=0	1000100	J68	SET ROSAR 11 IF SAL00-07 = 0.	DS121
R	TCS/ST	1000101	J69	SET ROSAR 11 IF INTERRUPT OR TIME CLOCK STEP OR STOP TGR=1.	DS122

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
R	3<STC	1000111	J71	SET ROSAR 11 IF STC GREATER THAN 011.	DS121
R	J47=1	1010000	J80	SET ROSAR 11 IF PAL32-62 = 0 AND PAL63=1.	DS111
R	STAA	1010001	J81	SET ROSAR 11 IF STAA = 1.	DS113
R	DECDIV	1010010	J82	SET ROSAR 11 IF DECIMAL DIVIDE OPERATION.	DS131
R	ΔTIC	1010011	J83	SET ROSAR 11 IF (TIC OR GAP OR UT BIT) AND NOT REPEAT FLT.	DS131
R	STAF=C	1010100	J84	SET ROSAR 11 IF STAF = STAC (SIGNS ALIKE).	DS113
R	ROS-PB	1010101	J85	SET ROSAR 11 IF ROS TRANSFER PUSHBUTTON ON.	DS122
R	JCRY4	1010110	J86	SET ROSAR 11 IF A CARRY EXISTS INTO PAL4 DURING FLPT OP.	DS151
R	DREG(18-23)	1100000	J96	SET ROSAR 09 IF D18-21=0. SET ROSAR 10 IF D22=1. SET ROSAR 11 IF D23=1.	DS051 DS061 DS075
R	* NEXT INST*IC	1100001	J97	SET ROSAR 06 IF EFFECTIVE R00=1. SET ROSAR 07 IF EFFECTIVE R01=1. SET ROSAR 08 IF EFFECTIVE RX FORMAT AND R12-15 = 0000. SET ROSAR 09 IF NOT EFFECTIVE RR FORMAT AND 4 BITS OF Q SELECTED BY IC21, 22 = 0000. SET ROSAR 10 IF IC21=1. SET ROSAR 11 IF IC22=1.	DS217 DS217 DS217 DS011, RX091 DS217 DS101

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
R	DECIMAL	1100010	J98	SET ROSAR 09 IF E12-15 = 0000.	DS051
				SET ROSAR 10 IF E08-11 = 0000 OR STC = 000.	DS061
				SET ROSAR 11 IF ABC DOES NOT = 000 OR E12-15 = 0000.	DS071,DS101
R	IC(21-22)	1100011	J99	SET ROSAR 10 IF IC21=1.	DS061
				SET ROSAR 11 IF IC22=1.	DS075
R	W1=(01-15)	1100100	J100	SET ROSAR 10 IF SAL04-07 = 1 THRU 4 OR 10 THRU 15.	DS061
				SET ROSAR 11 IF SAL04-07 = 5 THRU 9 OR 10 THRU 15.	DS101
R	STAE,F1SGN+	1100101	J101	SET ROSAR 10 IF STAE = 1.	DS061
				SET ROSAR 11 IF F04-07 = PLUS SIGN.	DS075
R	E(04-07)-ROA	1100110	J102	SET ROSAR 08 IF E04=1.	DS217
				SET ROSAR 09 IF E05=1.	DS217
				SET ROSAR 10 IF E06=1.	DS061
				SET ROSAR 11 IF E07=1.	DS071
R	E(02-07)-ROA	1100111	J103	SET ROSAR 06 IF E02=1.	DS217
				SET ROSAR 07 IF E03=1.	DS217
				SET ROSAR 08 IF E04=1.	DS217
				SET ROSAR 09 IF E05=1.	DS217
				SET ROSAR 10 IF E06=1.	DS217
				SET ROSAR 11 IF E07=1.	DS071

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
R	EDIT	1101000	J104	SET ROSAR 09 IF ABC = 111.	DS051
				SET ROSAR 10 IF E08-15 = 0000 OR STC = 111.	DS065
				SET ROSAR 11 IF E07=1 AND EDIT AND MARK LATCH = 1.	DS075
R	FLPT-UN,COMP	1101001	J105	SET ROSAR 10 IF FLTG. PT. UNNORMALIZED OPERATION.	DS061
				SET ROSAR 11 IF FLTG. PT. COMPARE OPERATION.	DS075
R	ΔW(01-02)	1101010	J106	SET ROSAR 10 IF SAL BIT 01 IS ON.	DS041
				SET ROSAR 11 IF SAL BIT 02 IS ON.	DS101
R	LOGIC-COMP	1101011	J107	SET ROSAR 09 IF SAL00-07 = 0.	DS051
				SET ROSAR 10 IF (ABC = 111 AND SAL00-07 = 0) OR (SAL00-07 DOES NOT = 0 AND CARRY OUT OF S ADDER).	DS065
				SET ROSAR 11 IF STC = 111 OR E08-15 = 0.	DS071,DS075
R	STAD,STAG	1101100	J108	SET ROSAR 10 IF STAD=1.	DS061
				SET ROSAR 11 IF STAG=1	DS075
R	J1=0/1,J18=0	1101101	J109	SET ROSAR 10 IF PAL 07-11 = 0 OR PAL06, 08-11 = ALL ONES,	DS065
				SET ROSAR 11 IF PAL 07-67 = 0.	DS075
R	SAS2,3,4	1101110	J110	SET ROSAR 09 IF SCAN ADDRESS SEQUENCER 2 = 1.	DS051
				SET ROSAR 10 IF SCAN ADDRESS SEQUENCER 3 = 1.	DS061
				SET ROSAR 11 IF SCAN ADDRESS SEQUENCER 4 = 1.	DS075

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
R	J1=0,J17=0	1101111	J111	SET ROSAR 10 IF PAL 08-15=0. SET ROSAR 11 IF PAL 07-63=0.	DS365 DS075
R	FLR	1111000	J120	SET ROSAR 08 IF CARRY OUT OF SERIAL ADDER (STAH NOT USED). SET ROSAR 09 IF STAC = STAF. SET ROSAR 10 IF FLTG. PT. CHARACTERISTIC DIFFERENCE IS NOT GREATER THAN 8 FOR SHORT OR NOT GREATER THAN 16 FOR LONG. SET ROSAR 11 IF SAL00-07=0.	DS365 DS051 DS065 DS071
R	* NEXT-INST*D	1111001	J121	SET ROSAR 06 IF EFFECTIVE R00=1. SET ROSAR 07 IF EFFECTIVE R01=1. SET ROSAR 08 IF EFFECTIVE RX FORMAT AND R12-15 = 0000. SET ROSAR 09 IF NOT EFFECTIVE RR FORMAT AND 4 BITS OF Q SELECTED BY D21, 22 = 0000. SET ROSAR 10 IF D21=1. SET ROSAR 11 IF D22=1.	DS217,RX091 DS217 DS217 DS215,RX091 DS065 DS101
R	J(58-63)	1111010	J122	SET ROSAR 09 IF PAL58-61 = 0000. SET ROSAR 10 IF PAL 62=1. SET ROSAR 11 IF PAL 63=1.	DS051 DS065 DS071
R	A1=0,J5=0	1111011	J123	SET ROSAR 10 IF A08-11 = 0000. SET ROSAR 11 IF PAL40-43 = 0000.	DS061 DS071

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
R	ALT,MS-TEST	1111100	J124	SET ROSAR 10 IF ALTERNATE TEST MUST BE FETCHED (FLT).	DS061
				SET ROSAR 11 IF TEST IS IN STORAGE (FLT).	DS073
R	Δ J47 \neq 0. Δ CRY Δ CRY	1111101	J125	SET ROSAR 10 IF NO CARRY FROM PAL 32 AND PAL 32-63 NOT ZERO.	DS041
				SET ROSAR 11 IF CARRY FROM PAL 32 AND PAL 32-63 NOT ZERO.	DS101

CONTROL FIELDS AND MICRO-ORDERS

K FIELD CONDITIONAL BRANCHES (ROSAR BIT 10) .
 THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 57-61.

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
R	0	00000	K0	RESET ROSAR 10 (UNCONDITIONAL).	
R	1	00001	K1	SET ROSAR 10 (UNCONDITIONAL).	DS201
R	E3=15	00010	K2	SET ROSAR 10 IF E12-15 = 1111.	DS205
R	E2=0/	00011	K3	SET ROSAR 10 IF E08-11 INCR LATCHES = 0000 OR STC = 000.	DS205
R	E2=15	00100	K4	SET ROSAR 10 IF E08-11 = 1111.	DS205
R	STAD	00101	K5	SET ROSAR 10 IF STAD = 1.	DS205
R	D(21)	00110	K6	SET ROSAR 10 IF D21 = 1.	DS205
R	↳RRS	00111	K7	SET ROSAR 10 ON RESTART TIMEOUT SIGNAL.	DS171
R	STAG	01000	K8	SET ROSAR 10 IF STAG = 1.	DS205
R	PSW39	01001	K9	SET ROSAR 10 IF PSW 39 = 1 (SIGNIFICANCE MASK).	DS205
R	DEC	01010	K10	SET ROSAR 10 IF E00-03 = 1111 (VFL DECIMAL).	DS205
R	STAE	01011	K11	SET ROSAR 10 IF STAE = 1.	DS205
R	┘RR.C	01100	K12	SET ROSAR 10 IF IC21-22 = 11 OR (NOT RR AND IC21-22 = 00).	DS161
R	W1=15	01101	K13	SET ROSAR 10 IF SAL 04-07 = 1111.	DS205
R	J47≠0	01110	K14	SET ROSAR 10 IF E07 = 0 AND PAL 32 NOT EOR FIXED PT. OVERFLOW (FAST PATH) OR IF E07 = 1 AND PAL 32 EOR FIXED PT. OVERFLOW OR IF E07 = 1 AND PAL 32-63 = 0.	DS261

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
R	W1=1	01111	K15	SET ROSAR 10 IF SAL 04-07 = 0001.	DS201
R	E23=0	10000	K16	SET ROSAR 10 IF E08-15 = 0000.	DS201
R	WCRY	10001	K17	SET ROSAR 10 IF CARRY OUT OF SERIAL ADDER (STAH NOT USED).	DS201
R	E=0/	10010	K18	SET ROSAR 10 IF E08-15 = 0000 OR STC = 111.	DS201
R	E3=0	10011	K19	SET ROSAR 10 IF E12-15 = 0000.	DS201
R	E3=0/	10100	K20	SET ROSAR 10 IF E12-15 = 0000 OR STC = 111.	DS201
R	INTRP	10101	K21	SET ROSAR 10 IF PROGRAM INTERRUPT.	DS201
R	F1≠1	10110	K22	SET ROSAR 10 IF F04-07 DOES NOT = 1.	DS201
R	F1≠9	10111	K23	SET ROSAR 10 IF F04-07 DOES NOT = 9.	DS201
R	T-RAR	11000	K24	INHIBIT ROSAR AND SET ROSAR 00-11 TO T40-51 (SCAN).	DS211
R	EXCEP	11001	K25	INHIBIT ROSAR IF EXCEPTION INTERRUPT AND FORCE ADDRESS TO ROSAR PER SOURCE OF EXCEPTION.	DS208
R	6 < E23	11010	K26	SET ROSAR 10 IF E08-15 IS GREATER THAN 6.	DS205
R	MOVE	11011	K27	SET ROSAR 10 IF MOVE OPERATION.	DS161
R	UFMSK	11100	K28	SET ROSAR 10 IF F01 = 1 AND PSW BIT 38 = 0 OR STAD = 0 AND PSW BIT 38 = 0 AND MULT OR DVD.	DS161
R	SPEC	11111	K31	INHIBIT ROSAR IF SPECIFICATION INTERRUPT AND FORCE ADDR 010 ROSAR. BLOCK LOCAL STORE WRITE.	DS261

CONTROL FIELDS AND MICRO-ORDERS

L FIELD MEMORY REQUESTS AND MARK SETTING .

THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 43-46.

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>AID</u>
		0000	L0	NO OPERATION	
S	STOP1	0001	L1	INHIBIT RISE OF NEXT P2 FOR 1 CYCLE (BUS NOT INHIBITED).	KC021
S	STOP2	0010	L2	INHIBIT RISE OF NEXT P2 FOR 2 CYCLES (BUS NOT INHIBITED).	KC021
S	▷ MS-REQ-LOG	0011	L3	REQUEST LOGOUT WORDS FROM STORAGE PER ABC.	DR181
S	SET-MARK-0-7	0100	L4	SET MARKS 0-7.	CT041
S	SET-MARK-0-3	0101	L5	SET MARKS 0-3.	CT021
S	SET-MARK*STC	0110	L6	SET MARKS PER STC.	CT011
S	SET-MARK*J61	0111	L7	SET MARKS 0-3 IF PAL61=0, SET MARKS 4-7 IF PAL61=1.	CT011
S	MS-REQ*IC-3	1000	L8	IC REQUESTS STORAGE (3 CYCLE).	DR181
S	MS-REQ*IC-4	1001	L9	IC REQUESTS STORAGE (4 CYCLE).	DR181
S	MS-REQ*D-3	1010	L10	D REQUESTS STORAGE (3 CYCLE).	DR181
S	MS-REQ*D-4	1011	L11	D REQUESTS STORAGE (4 CYCLE).	DR181
S	MS*IC-3*D=11	1100	L12	IF D21,22=3 IC REQUESTS STORAGE (3 CYCLE) AND TURN ON INSTRUCTION MEMORY FETCH TGR.	DR181 KD201
S	MS-REQ*SCAN4	1101	L13	SCAN REQUESTS STORAGE (4 CYCLE).	DR181
S	▷ RQ-XY-STO*D	1110	L14	REQUEST TO STORE XY REG. (REQUIRES SET MARKS).	DR185

CONTROL FIELDS AND MICRO-ORDERS

M FIELD SERIAL ADDER A SIDE CONTROLS .

THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 69-73.

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
B	+0	00000	M0	ZERO GATED WITH PARITY.	
B	+ΔDECAB	00100	M4	DECODE F REG BITS 05-07 TO SELECT BIT OF AB BYTE AND GATE SELECTED BIT TO SA06. GATE ZEROES TO SA00-05 AND 07.	AR421
B	-U,CRY	00101	M5	SBA00-07 COMP TO SA00-07, HOT CARRY TO SA07, IF CARRY OUT-SAVE IN STAH.	AR401 AR411
B	-ΔU	00111	M7	SBA00-07 COMP TO SA00-07, HOT CARRY TO SA07. 1 TO SA00 IF NOT 9020 OP.	AR411
B	?U*E1	01100	M12	AND FUNCTION IF E06-07=00, OR FUNCTION IF E06-07= 10, EXCLUSIVE OR FUNCTION IF E06-07= 11.	AR421
B	+U1,U0	01101	M13	SBA00-03 TO SA04-07, SBA04-07 TO SA00-03.	AR401
B	+U1,0	01111	M15	SBA04-07 L4 TO SA00-03 (SA04-07=0000).	AR401,AR411
B	+U0,0	10001	M17	SBA00-3 TO SA00-3 (SA04-07=0000).	AR401,AR411
B	.U	10010	M18	AND FUNCTION, SBA00-07 TO SA00-07.	AR421
B	+U	10011	M19	SBA00-07 TO SA00-07.	AR401
B	∇U	10100	M20	EXCLUSIVE OR FUNCTION, SBA00-07 TO SA00-07.	AR421
B	+15,U0	10101	M21	ZONE TO SA00-03 ((1111 IF PSW12=0, 0101 IF PSW12=1) BOTH SBA00-03 AND SBA00-03 COMP TO SA00-03 USED), SBA00-03 R4 TO SA04-07.	AR401,AR411

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
B	OU	10110	M22	OR FUNCTION, SBA00-07 TO SA00-07.	AR421
B	+15,U1	10111	M23	ZONE TO SA00-03 ((1111 IF PSW12=0, 0101 IF PSW12=1) BOTH SBA00-03 AND SBA00-03 COMP TO SA00-03 USED), SBA04-07 TO SA04-07.	AR401 AR411
B	+6U	11000	M24	SBA00-03+6 TO SA00-03, SBA04-07+6 TO SA04-07, SERIAL CARRY TO SA07, DECIMAL CORRECT 00-03, 04-07, SET STAA IF SUM NOT ZERO, SET STAE IF INVALID DIGIT, SET STAH IF CARRY, RESET STAH IF NO CARRY.	AR401 AR411
B	+6U0,0	11001	M25	SBA00-03+6 TO SA00-03 (SA04-07=0000), DECIMAL CORRECT 00-03, SET STAA IF SUM NOT ZERO 00-03, SET STAE IF INVALID DIGIT 00-03, SET STAH IF CARRY, RESET STAH IF NO CARRY.	AR401 AR411
B	+6U0,S	11010	M26	SBA00-03+6 TO SA00-03, CORRECT SIGN TO SA04-07 (1100 OR 1101 IF PSW12=0, 1010 OR 1011 IF PSW12=1), DECIMAL CORRECT 00-03, SET STAA IF SUM NOT ZERO 00-03, SET STAE IF INVALID DIGIT IN 00-03 OR INVALID SIGN IN 04-07. SET STAC IF SBA04-07 IS NEG SIGN. SET STAH IF CARRY, RESET STAH IF NO CARRY.	AR411
B	+0,U1	11011	M27	SBA04-07 TO SA04-07 (SA00-03=0000).	AR401 AR411
B	-U	11100	M28	SBA00-07 COMP TO SA00-07, SERIAL CARRY TO SA07, DECIMAL CORRECT 00-03, 04-07, SET STAA IF SUM NOT ZERO, SET STAE IF INVALID DIGIT.	AR401

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
B	+0,U0	11101	M29	SBA00-03 R4 TO SA04-07 (SA00-03=0000).	AR401
B	-U0,0	11110	M30	SBA00-03 COMP TO SA00-03 (SA04-07=0000), HOT CARRY TO SA03, DECIMAL CORRECT 00-03, SET STAA IF SUM NOT ZERO 00-03, SET STAE IF INVALID DIGIT 00-03.	AR411
B	+0,U	11111	M31	SBA01-07 TO SA01-07, 0 TO SA00.	AR411

CONTROL FIELDS AND MICRO-ORDERS

N FIELD SERIAL ADDER B SIDE CONTROLS .
 THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 74-77 .

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
B	0	0000	NO	ZERO GATED WITH PARITY.	AR901
B	V	0010	N2	SBB00-07 TO SB00-07.	AR901
B	0,V1	0011	N3	SBB04-07 TO SB04-07 (SB00-03=0000).	AR901
B	V0,+	0100	N4	PLUS SIGN TO SB04-07 (1100 IF PSW12=0, 1010 IF PSW12=1) SBB00-03 TO SB00-03.	AR901
B	QUOT	0101	N5	B66-67 TO 2 BITS OF SAL00-07 SELECTED BY MULTIPLE SET, QUOTIENT INSERTION ORDERS (FIELD G 20, 21).	AR901 AR901
B	0,V	0110	N6	SBB01-07 TO SB01-07, 0 TO SB00.	AR901
B	9,V1	0111	N7	1001 TO SB00-03 (EFFECTIVELY ADDS +9). SBB04-07 TO SB04-07.	AR901
B	-64	1000	N8	11000000 TO SB00-07 (EFFECTIVELY ADDS -64).	AR901
B	V0,0	1010	N10	SBB00-03 TO SB00-03 (SB04-07=0000).	AR901
B	-1	1011	N11	11111111 TO SB00-07 (EFFECTIVELY ADDS -1).	AR901
B	V0,-	1100	N12	MINUS SIGN TO SB04-07 (1101 IF PSW12=0, 1011 IF PSW12=1) SBB00-03 TO SB00-03.	AR901
B	V0,V0	1110	N14	SBB00-03 TO BOTH SB00-03 AND SB04-07.	AR901
B	1	1111	N15	00000001 TO SB00-07 (EFFECTIVELY ADDS +1).	AR901

CONTROL FIELDS AND MICRO-ORDERS

P FIELD PARALLEL ADDER LATCH CONTROL.

THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 78-80.

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
A	→	000	P0	PADDER 04-67 TO PAL04-67 (NO SHIFT).	AP821
A	SCAN-BYPASS	001	P1	PADDER 04-31, 64-67 TO PAL 04-31, 64-67 (NO SHIFT) SCAN OUT BUS32-63 TO PAL 32-63 (ENABLE SCAN BYPASS).	AP821
A	R→	010	P2	PADDER 04-63 R4 TO PAL 08-67 (PADDER 04 PROPAGATES INTO PAL04-08).	AP821
A	→HOLD	100	P4	HOLD VALUE IN PAL 04-67 FOR 1 CYCLE.	AP821
A	L→	101	P5	PADDER 08-67 L4 TO PAL 04-63 (0000 TO PAL 64-67).	AP821
A	,C8	110	P6	PB64-67 2's COMPLIMENT TO PADDER 64-67, PADDER 64-67 TO PAL64-67 (NO SHIFT), IF PB64-67 ≠ 0 BLOCK HOT CARRY TO PA63.	AP821
A	ΔR1→	111	P7	PADDER 32-63 R1 TO PAL 33-64, ZEROES TO PAL 32 AND 48.	AP821

CONTROL FIELDS AND MICRO-ORDERS

Q FIELD HOT ONES TO PARALLEL ADDER A SIDE.
 THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 82-84.

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
		000	Q0	NO OPERATION.	
A	+P	001	Q1	HOT ONES TO PA26-31 (FOR FIXED-PT NON- LOGICAL OPS PROPAGATES SIGN (T32) PER TRUE OR COMP OPERATION).	AP731
A	+8	010	Q2	HOT ONE TO PA60 (EFFECTIVELY ADDS +8).	AP811
A	+1	011	Q3	HOT CARRY TO PA63 (BLOCKED IN CONVERT TO DECIMAL IF SAL 00=0).	AP737
A	-16	100	Q4	HOT ONES TO PA32-59 (EFFECTIVELY ADDS -16).	AP811
A	+TIME	101	Q5	HOT ONES TO PA32-52, 54, 55 (FOR TIME CLOCK UPDATE).	AP811
A	-8	110	Q6	HOT ONES TO PA32-60 (EFFECTIVELY ADDS -8).	AP811
A	-1	111	Q7	HOT ONES TO PA32-63 (EFFECTIVELY ADDS -1).	AP811

CONTROL FIELDS AND MICRO-ORDERS

R FIELD OUTGATES TO SERIAL ADDER INBUS A SIDE.
 THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 86.

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
B	AB→U	0	R0	AB BYTE (SELECTED BY ABC) TO SBA00-07.	RB801
B	F→U	1	R1	F00-07 TO SBA00-07.	RF801

CONTROL FIELDS AND MICRO-ORDERS

T FIELD OUTGATES TO PADDR B SIDE FROM A,B,IC.
 THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 87-90.

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
A	0	0000	T0	ZERO GATED WITH PARITY	RB755 RB757 RB761
A	BL2	0001	T1	B32-67 L2 TO PB30-65 (PB66,67 = 00) IF FXP MPY, PROPAGATE SIGN (B32 TO PB28,29).	RB811
A	IC	0010	T2	IC00-23 TO PB40-63.	RB811
A	DEC	0011	T3	GENERATES EXCESS 6 DECIMAL CORRECTION FACTOR TO PB28-63 FOR CONVERT TO DECIMAL (WITH FIELD U6).	RB805
A	F1	0100	T4	F04-07 TO PB60-63.	RB807
A	ABL2	0101	T5	AB06-67 L2 TO PB04-65 (PB66,67 = 00) (A05 MUST BE EVEN PARITY).	RB811
A	8	0110	T6	HOT ONE TO PB60 (EFFECTIVELY ADDS +8).	RB807
A	B8J9	0111	T7	B64-67 TO PB28-31.	RB807
A	A	1000	T8	A00-31 TO PB32-63.	RB805
A	B8	1001	T9	B64-67 TO PB64-67.	RB813
A	A13	1010	T10	A08-31 TO PB08-31.	RB813
A	B	1011	T11	B32-63 TO PB32-63.	RB813
A	AB	1100	T12	AB04-67 TO PB04-67 (A00-03 MUST BE ZERO).	RB805
A	Δ2	1101	T13	HOT ONE TO PB62 (EFFECTIVELY ADDS +2).	RB807

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
A	AB17	1110	T14	AB08-63 TO PB08-63.	RB813
A	B489	1111	T15	B32-63 TO PB32-63, B64-67 TO PB28-31.	RB807
A	AB18	1110	T14	AB08-67 TO PB08-67 (FL PT ADD, SUB OR COMP).	RB813

CONTROL FIELDS AND MICRO-ORDERS

U FIELD OUTGATES TO Padder A SIDE FROM S, T, AND D.
 THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 96,92-95.

EDGE CHAR	MICRO-ORDER	BITS 96 92 95	DEC ORDER	FUNCTION	ALD
A	+0	00000	U0	ZERO GATED WITH PARITY.	
A	-TL1	00001	U1	T32-63 COMP L1 TO PA31-62 (1 + HOT CARRY TO PA63).	RT811
A	-D	00010	U2	D00-23 COMP TO PA40-63 (HOT CARRY TO PA63), INSERT ONES TO PA32-39.	RT801
A	+D	00011	U3	D00-23 TO PA40-63.	RT801
A	+S	00100	U4	S00-31 TO PA32-63.	RT815
A	-DTL1	00101	U5	ONES TO PA04-06, D00-23 COMP L1 TO PA07-30, T32-63. COMP L1 TO PA31-62 (1 + HOT CARRY TO PA63).	RT805 RT811
A	+TL1	00110	U6	T32-63 L1 TO PA31-62 (PA63=0).	RT811
A	+DTL1	00111	U7	D00-23 L1 TO PA07-30, T32-63 L1 TO PA31-62 (PA63=0).	RT805 RT811
A	+T45R	01000	U8	T32-47 TO PA48-63, 1 TO PA47 IF T32=0.	RT813
A	+T67	01001	U9	T48-63 TO PA48-63, 1 TO PA47 IF T48=0.	RT815
A	-D+7	01010	U10	D00-23 COMP TO PA40-63 (HOT CARRY TO PA63), OR ONES INTO PA61-63, INSERT ONES TO PA32-39.	RT801 RT813
A	+DJ13	01011	U11	D00-23 TO PA08-31.	RT803
A	-DT	01100	U12	ONES TO PA04-07, D00-23 TO PA08-31 COMP, T32-63 COMP TO PA32-63 (HOT CARRY TO PA63).	RT803 RT807

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
A	-T	01101	U13	T32-63 COMP TO PA32-63 (HOT CARRY TO PA63).	RT807
A	+T	01110	U14	T32-63 TO PA32-63.	RT807
A	+DT	01111	U15	D00-23 TO PA08-31, T32-63 TO PA32-63.	RT803,RT807
A	+ΔK	10000	U16	K00-31 TO PA32-63.	RT817
D	ΔFMTO*E13-15	10001	U17	FORMAT IM REG TO XY REG (HISTORY) PER E13-15.	RT843
D	ΔFMFN*E13-15	10010	U18	FORMAT LM REG TO XY REG (CSS-NEW) PER E13-15.	RT843
D	ΔFMFW*E14-15	10011	U19	FORMAT IM REG TO XY REG (WEATHER) PER E14-15.	RT843
A	+Δ2	10100	U20	HOT ONE TO PA62 (EFFECTIVELY ADDS +2).	RT841
A	+Δ32	10101	U21	HOT ONE TO PA58 (EFFECTIVELY ADDS +32).	RT841
A	+ΔT45R	11000	U24	T32-47 TO PA48-63.	RT813
A	+ΔT67	11001	U25	T48-63 TO PA48-63.	RT815

CONTROL FIELDS AND MICRO-ORDERS

V FIELD E AND Q REGISTERS TO PARALLEL ADDER B-SIDE .
 THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 97-99.

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
	0	000	V0	ZERO GATED WITH PARITY.	
A	E3	001	V1	E12-15 TO PB60-63.	RQ801
A	E2	010	V2	E08-11 TO PB60-63.	RQ801
A	E23	011	V3	E08-15 TO PB56-63.	RQ801
A	Q7	100	V4	Q52-63 TO PB52-63.	RQ811
A	Q5	101	V5	Q36-47 TO PB52-63.	RQ811
A	Q3	110	V6	Q20-31 TO PB52-63.	RQ811
A	Q1	111	V7	Q04-15 TO PB52-63.	RQ811

CONTROL FIELDS AND MICRO-ORDERS

W FIELD FAA AND MISC CONTROL LINES,
THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 02-05.

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
	0	0000	W0	NO OPERATION.	
C	Δ13→ADR-SQCR	0001	W1	SET SCAN ADDRESS SEQUENCER TO 13.	DR011
C	ΔLMT1	0010	W2	RESET LIMIT LATCH, THEN SET LIMIT LATCH IF NO CARRY FROM EITHER PADDER BIT 32 OR 48.	DR011
C	ΔLMT2	0011	W3	SET LIMIT LATCH IF CARRY FROM EITHER PADDER BIT 32 OR 48.	DR011
C	SAMPLEΔVALUE	0100	W4	SAMPLE TO SE-DE ASSIGNMENT COMPARATOR ON BITS 0-3 OF F REG ON SATR. CHECK A REG 02-05 FOR VALID CE ON SCON.	DR011
D	ΔMS→LM	0101	W5	SDBO 00-63 TO LM REG 00-63.	DR011
L	* RΔATR2	1000	W8	GATE ADDRESS TRANSLATION REGISTER SECTION 2 TO L.S. BUSS.	DR011
D	ΔLOAD-REG	1001	W9	T REG TO ATR OR PSBAR, OR EXTERNAL REG TO CCR PER REGISTER SELECTION SWITCH.	DR011
B	** ΔNO→V	1010	W10	GATE N00-07 TO SERIAL ADDER B SIDE 00-07.	DR011
L	* RΔGREG	1011	W11	GATE G 00-07 TO L.S. BUSS BITS 24-31.	DR011
L	* RΔEXTBUS	1100	W12	GATE EXTERNAL BUSS TO L.S. BUSS.	DR011

* THESE MICRO-ORDERS ALSO ACTIVATE H64 MICRO-ORDER.

** THESE MICRO-ORDERS ALSO ACTIVATE E16 MICRO-ORDER.

CONTROL FIELDS AND MICRO-ORDERS

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
L	Δ GEN-BUS-PAR	1101	W13	GENERATE LOCAL STORE BUSS PARITY.	DR011
B	** Δ N1 \rightarrow V	1110	W14	GATE N08-15 TO SERIAL ADDER B SIDE 00-07.	DR011
D	Δ T \rightarrow M	1111	W15	GATE T 32-63 TO LM 32-63.	DR011

**THESE MICRO-ORDERS ALSO ACTIVATE E16 MICRO-ORDER.

CONTROL FIELDS AND MICRO-ORDERS

S FIELD SCAN MODE SPECIAL CONTROL LINES .

THE FOLLOWING MICRO-ORDERS ARE LOCATED IN BITS 17-19, 25-30, 31-35.

<u>EDGE</u> <u>CHAR</u>	<u>MICRO-ORDER</u>	<u>BITS</u>	<u>DEC</u> <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
<u>BITS 17-19 (SD FIELD)</u>					
C	ADRSQNCR-1	010	SD2	SUB 1 FROM ADDRESS SEQUENCERS.	DR201
C	Δ16→ADR-SQCR	011	SD3	SET ADDRESS SEQUENCER TO 16.	DR201
C	Δ15→ADR-SQCR	100	SD4	SET ADDRESS SEQUENCERS TO 15.	DR201
D	MSK-ADR→SAB	101	SD5	GATE MASK ADDRESS TO SAB.	DR201
D	SCANOUT-SREG	110	SD6	SCAN OUT S REG.	DR201
<u>BITS 25-30 (SF FIELD)</u>					
C	1-CTRCTL-TGR	000001	SF1	SET SCAN COUNTER CONTROL TGR.	DR201
C	STOP.1-UNCND	000100	SF4	STOP SCAN AND TON UNCONDITIONAL TERMINATION.	DR201
C	0→TIC,GAP	000101	SF5	RESET TIC AND GAP LATCHES.	DR201
C	1-MCH-CK TRP	000110	SF6	SET MACHINE CHECK INTERRUPT.	DR201
D	SCANOUT-TREG	000111	SF7	SCAN OUT T REG.	DR201
C	0→PASS/FAIL	001000	SF8	RESET PASS OR FAIL TGRS.	DR201
<u>BITS 31-35 (SG FIELD)</u>					
D	SCANOUT-RTWD	00001	SG1	SCAN OUT RIGHT INDICATOR WORD.	DR201
D	SCANOUT-LTWD	00100	SG4	SCAN OUT LEFT INDICATOR WORD.	DR201
C	1→PASS/FAIL	01000	SG8	SET PASS OR FAIL TGRS.	DR201
C	ΔINVERT-BFR1	01001	SG9	INVERT THE BUFFER 1 TGR.	DR201
C	FLTΔINITLIZE	01010	SG10	INITIALIZE AT START OF RECORD.	DR201
C	Δ7→ADR-SQCR	01011	SG11	SET ADDRESS SEQUENCERS TO 7.	DR201

CONTROL FIELDS AND MICRO-ORDERS

EDGE CHAR	<u>MICRO-ORDER</u>	<u>BITS</u>	DEC <u>ORDER</u>	<u>FUNCTION</u>	<u>ALD</u>
C	Δ MACH-RESET	01100	SG12	MACHINE RESET.	DR201
C	0→SCAN-MODE	01101	SG13	RESET SCAN MODE TGR.	DR201
D	SCAN-IN	01110	SG14	SCAN IN.	DR201
C	Δ 23→ADR-SQCR	01111	SG15	SET ADDRESS SEQUENCERS TO 23.	DR201

NOTE: SCAN MODE TGR ON DR211.

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